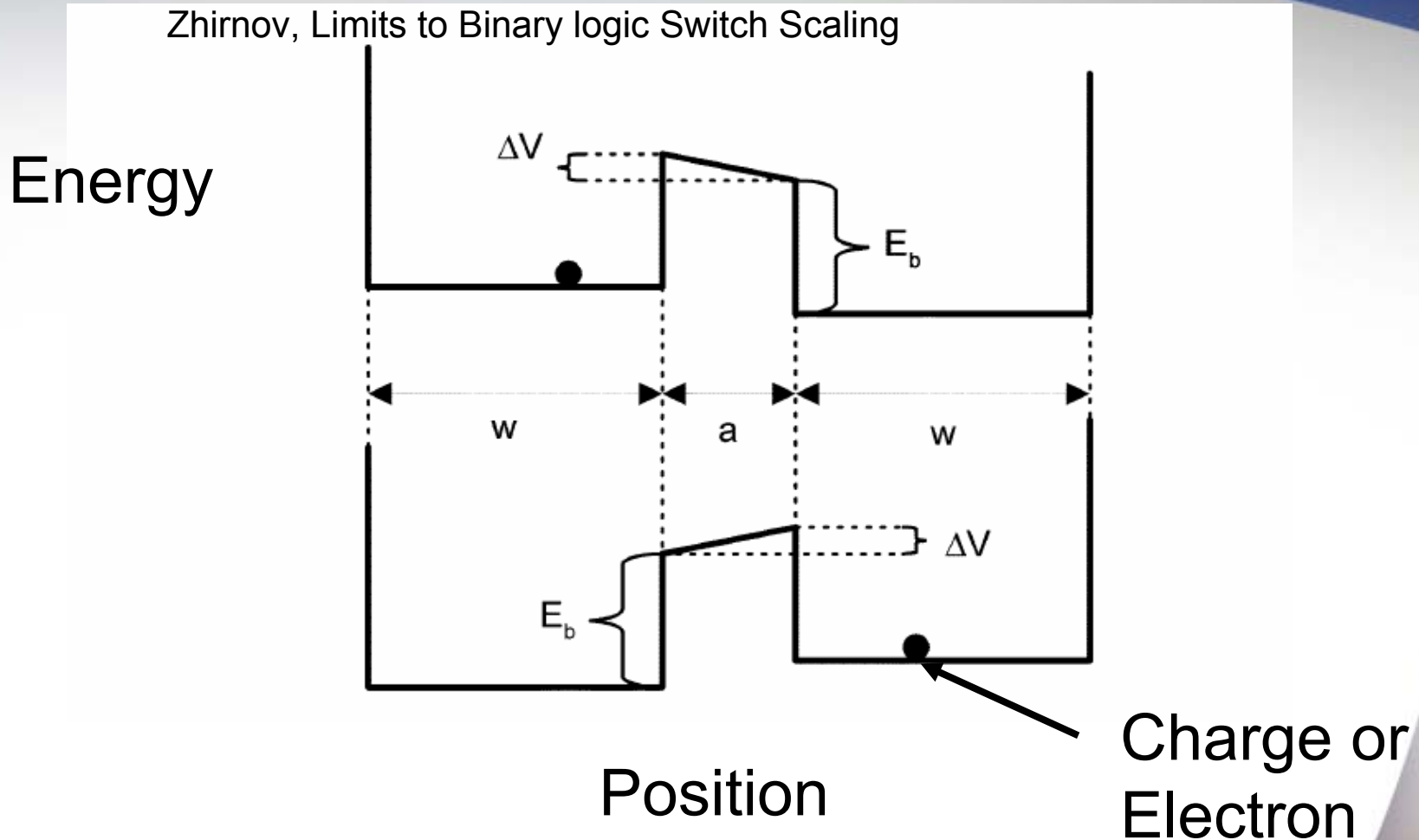


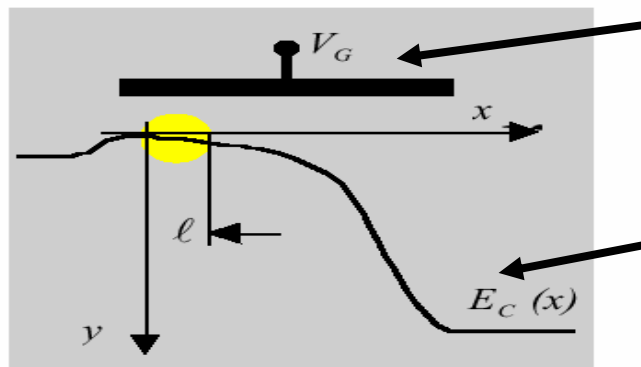
# Is This a Practical Device ?



What are some requirements that information is not lost?

# Lecture : 4

## Limits for Si MOSFETs



Gate lowers barrier

Drain voltage causes charge to move

Fig. 1 The conduction band edge vs. position from the source to the drain of a nanoscale MOSFET under high gate and drain bias.

Lundstrom, Essential Physics of Carrier Transport in Nanoscale MOSFETs

# Outline

- Performance limit (today)
- Power limit (future lecture)

# Some Papers

Keyes, Fundamental limits of Silicon Technology

Assad, On The Performance Limits of Si MOSFETS

Zhirnov, Limits to Binary Logic Switch Scaling

Assad, Performance limits of Silicon MOSFET

## On the Performance Limits for Si MOSFET's: A Theoretical Study

Farzin Assad, Zhibin Ren, Dragica Vasileska, *Member, IEEE*, Supriyo Datta, *Fellow, IEEE*, and Mark Lundstrom, *Fellow, IEEE*

*Abstract*—Performance limits of silicon MOSFET's are examined by a simple analytical theory augmented by self-consistent Schrödinger–Poisson simulations. The on-current, transconductance, and drain-to-source resistance in the ballistic limit (which corresponds to the channel length approaching zero) are examined.

Before we begin, we should discuss the limits discussed here are of course. Hot electrons near the drain have a few Angstroms, much shorter than the channel length of present-day MOSFET's. But

Information itself as an abstract construct. Processing, storing, and transmitting information requires that it be represented as the value of some physical quantity. Physical laws do control the material devices that are used to manipulate information; in other words, information processing technology. The purpose of this review is to use physics to discover where limits to continued advances of the

## Limits to Binary Logic Switch Scaling— Gedanken Model

VICTOR V. ZHIRNOV, RALPH K. CAVIN, III, FELLOW, IEEE,  
JAMES A. HUTCHBY, SENIOR MEMBER, IEEE, AND GEORGE I. BOURIANOFF, MEMBER, IEEE

*Invited Paper*

## Performance Limits of Silicon MOSFET's

Farzin Assad, Zhibin Ren, Supriyo Datta, and Mark Lundstrom  
Purdue University, West Lafayette, IN USA 47907-1285

Peter Bendix  
LSI Logic Corporation, Milpitas, CA 95035

### Abstract

A procedure for comparing the current vs. voltage characteristics of MOSFETs against their upper limits is presented, and a 0.35  $\mu\text{m}$  n-MOS technology is assessed. The effect of channel back-scattering coefficients for this technology are

this degenerate Fermi gas depends on the carrier occupancies and is readily calculated. The carrier velocity at the source approaches the thermal velocity when few of the thermal carriers are scattered back to the beginning of the channel by channel back-scatter to the beginning of the channel. The on-current of a nanoscale MOSFET

# How MOSFET Works

## (or In General a Charge Based Device)

- Switch control by a third terminal
  - Why is that important?
- Gate controls potential barrier that
  - control the flow of electrons
- Logic operation: electrons transferred
  - from a voltage source to capacitors
  - from capacitors to ground.
- Flow of electrons from power supply to ground dissipates energy

# Why A Charge Control Device

- Signals easily distributed throughout the system. Change moved via metal wires
- High gain
  - supplies a forgiving environment
- Immune to many sources of variation
  - temperature,
  - mechanical strain,
  - diffusion profiles
  - Many other
- Easy to handle Fan-out (larger W)

# MOSFET Performance limit

$$L_E \rightarrow 0$$

$T_{OX} \rightarrow$  Tunneling Limit

# Standard MOSFET Equation

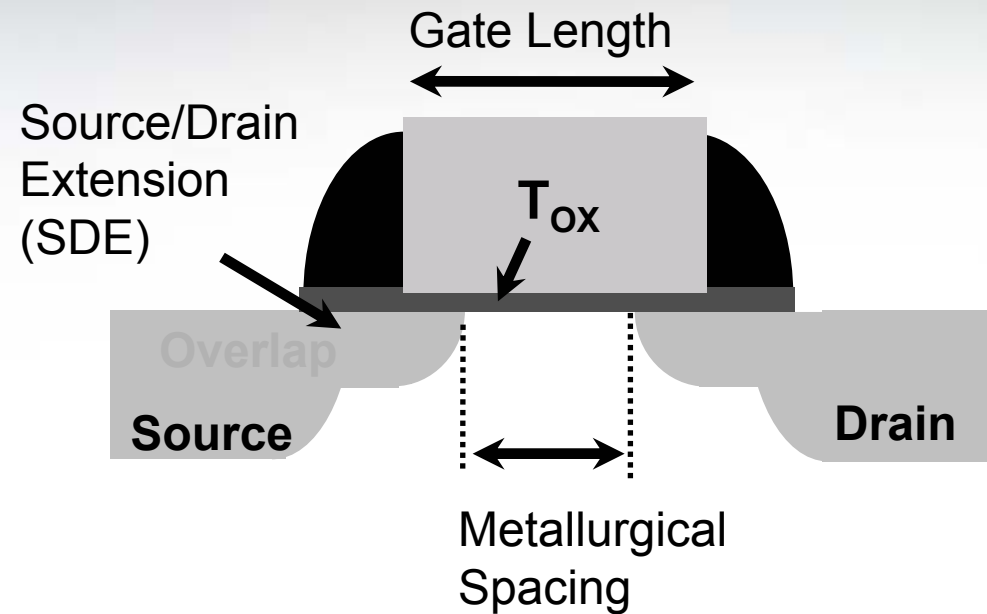
$$I_D = \mu \cdot C_{OX} \cdot \frac{W}{L} \cdot (V_{GS} - V_T) \cdot V_{DS}, \text{ for } |V_{DS}| \ll (V_{GS} - V_T)$$

$$I_D = \mu \cdot C_{OX} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - \frac{V_{DS}}{2}) V_{DS}, \text{ for } V_{DS} < (V_{GS} - V_T)$$

$$I_D = \mu \cdot C_{OX} \cdot \frac{W}{L} \cdot \frac{(V_{GS} - V_T)^2}{2}, \text{ for } V_{DS} \geq (V_{GS} - V_T)$$

What happens in limit  $L \rightarrow 0$ ?

# Constant Field Scaling Theory



Constant field

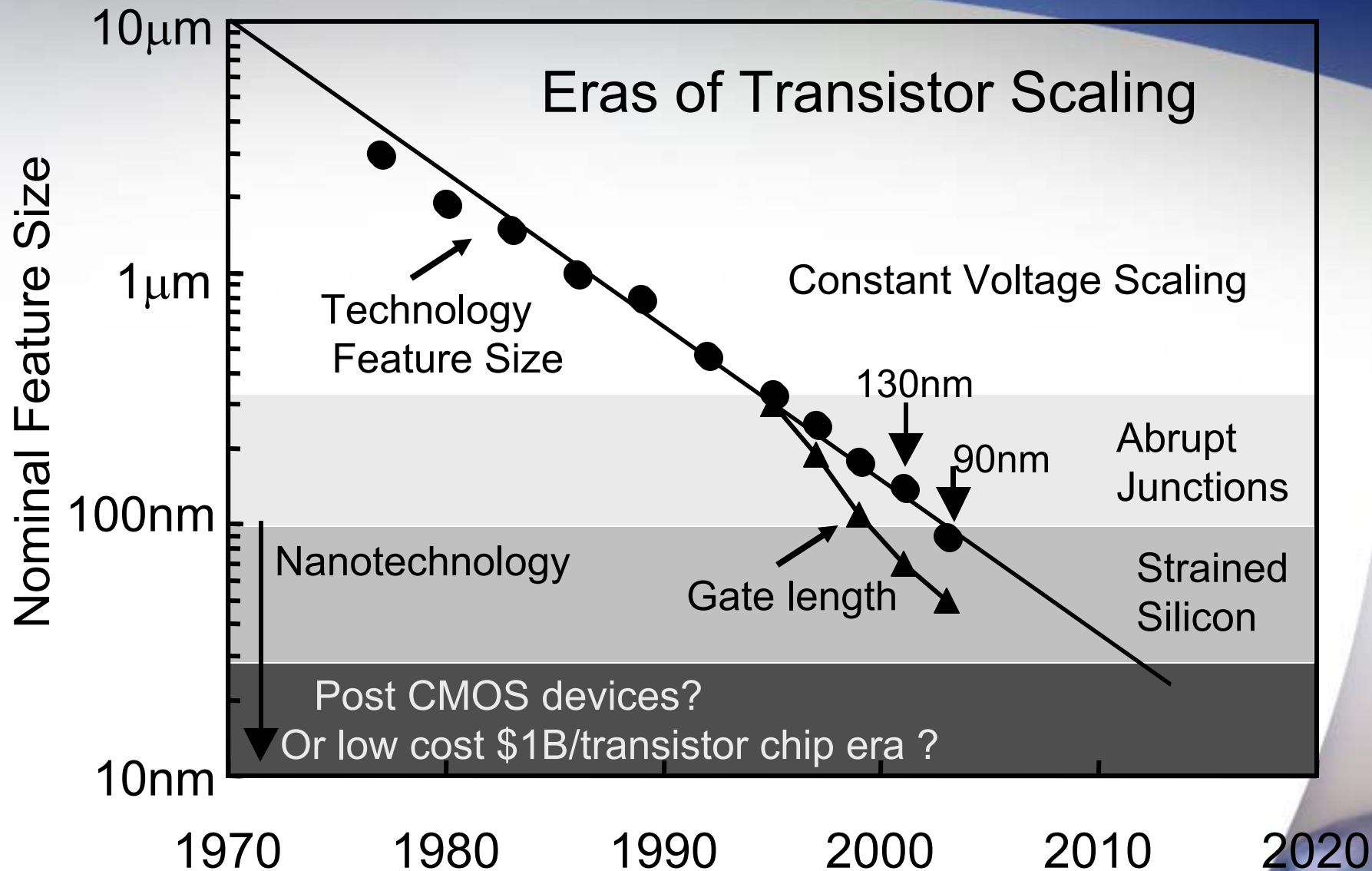
$\lambda = k$

Dimension	$\lambda$	$k$
Potential	$k$	$k$
Impurity Con.	$k/\lambda^2$	$1/k$
Electric Field	$k/\lambda$	<b>1</b>
$C_{ox}$	$\lambda$	$k$
Current	$k^2/\lambda$	$k$
Power	$k^3/\lambda$	<b><math>k^2</math></b>
Power * delay	$\lambda^2/k$	<b><math>k</math></b>

$k$  = voltage scale factor

$\lambda$  = linear dimension scale factor

# Eras of Transistor Scaling



# So What Happens to MOSFET drive current?

$$L_E \rightarrow 0$$

$T_{OX} \rightarrow$  Tunneling Limit

infinity ?

# Alternate MOSFET Description (A Simple Ballistic Picture)

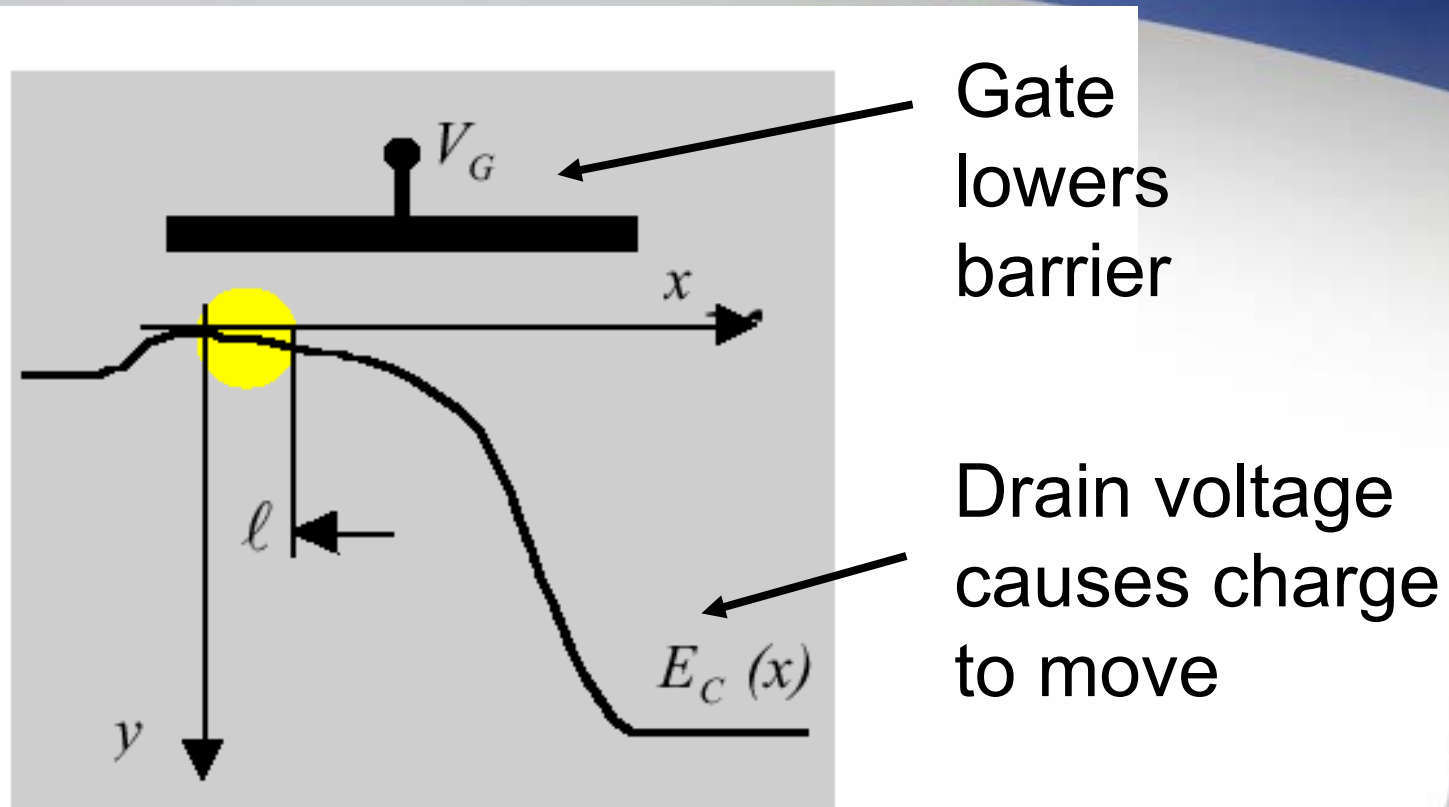


Fig. 1 The conduction band edge vs. position from the source to the drain of a nanoscale MOSFET under high gate and drain bias.

Lundstrom, Essential Physics of Carrier Transport in Nanoscale MOSFETs

# Ballistic Limit

- Simple ballistic picture: The mean free path being much larger than channel length
- Ballistic limit corresponds to the channel length approaching zero
- No scattering before traveling distance  $\ell$  which drops  $kT/q$  potential.
  - Scattering after dropping  $kT/q$  unlikely to emerge from the channel at source
- 0.35 $\mu\text{m}$  devices operate at  $\sim 1/2$  ballistic limit (IEDM Lundstrom)

# Fluid Flow Analogy

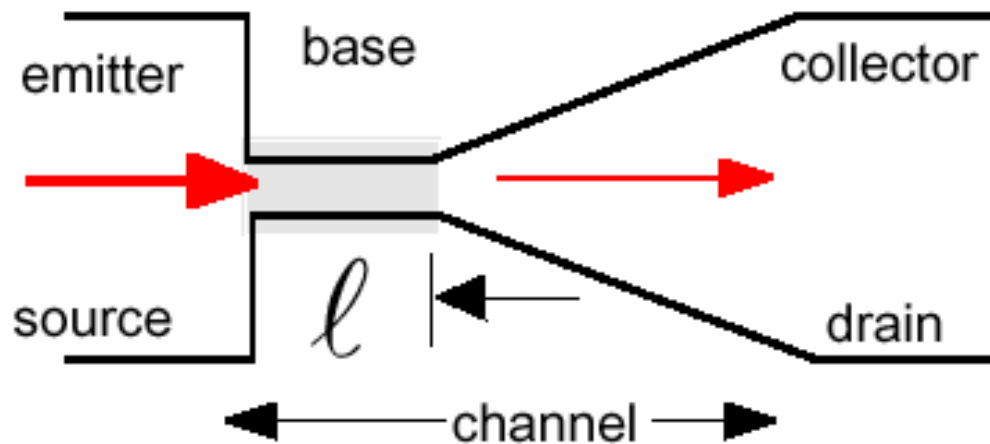


Fig. 2 A fluid flow analogy for the MOSFET under high gate and drain bias conditions.

Lundstrom, Essential Physics of Carrier Transport in Nanoscale MOSFETs

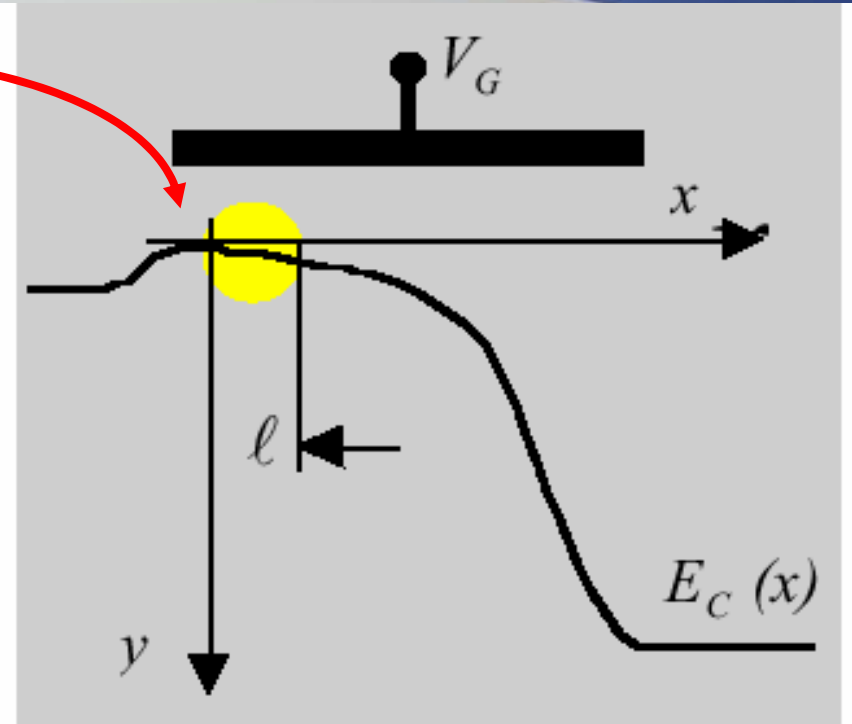
# Alternate MOSFET Description Equations

$$q n_s(0) \approx C_{ox} (V_{GS} - V_T),$$

$$I_D = W C_{ox} \langle v(0) \rangle (V_{GS} - V_T),$$

$$\langle v(0) \rangle = \left( \frac{1-r}{1+r} \right) v_T$$

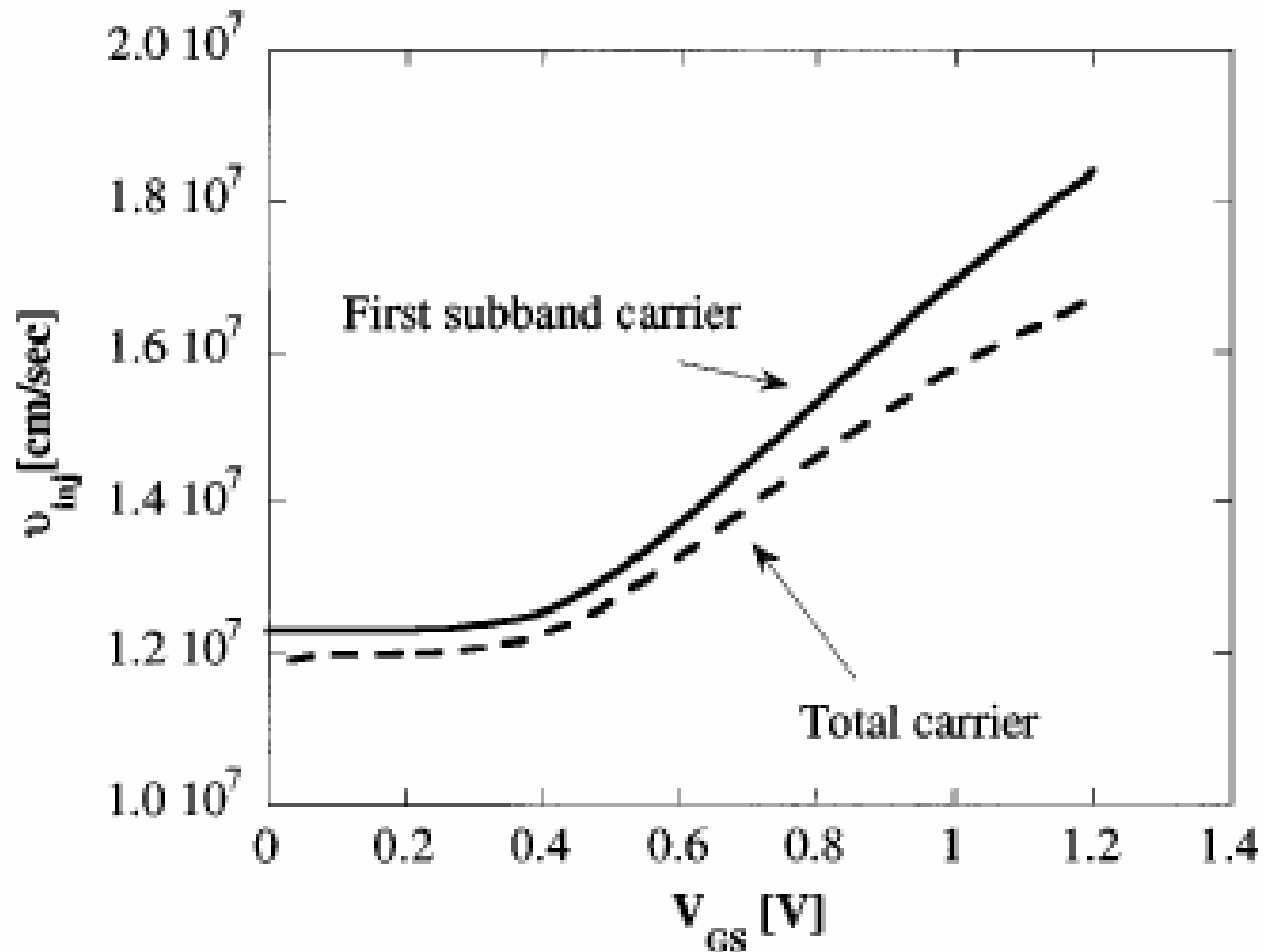
$$v_T = \sqrt{\frac{2k_B T_L}{\pi m_i^*}} \left\{ \frac{\mathcal{F}_{1/2}(\eta)}{\ln(1+e^\eta)} \right\},$$



$V_T$  = thermal velocity

$r$  = backscattering coefficient

# Thermal Velocity



# Class Example On Board

# Results in Paper

Production  
today

ID= 1250

Intel 65nm  
2004 IEDM  
paper?

ID= 1450

TABLE I  
COMPUTED PERFORMANCE OF THE MODEL BALLISTIC  
DEVICE AT 300K. THE THRESHOLD VOLTAGE WAS  $-0.4$  V, THE GATE  
OVERDRIVE WAS  $(V_{GS} - V_T) = 0.8$  V, AND THE DRAIN VOLTAGE WAS 1.0 V

Gate	$I_D$ ( $\mu\text{A}/\mu\text{m}$ )	$g_m$ (mS/mm)	$g_m/I_D$ ( $\text{V}^{-1}$ )	$R_i$ ( $\Omega\text{-}\mu\text{m}$ )
Metal	2200	3500	1.7	44
Polysilicon	1700	2800	1.7	52

TABLE II  
COMPUTED PERFORMANCE OF THE MODEL BALLISTIC DEVICE AT 77K. THE  
THRESHOLD VOLTAGE WAS  $-0.5$  V AND THE GATE OVERDRIVE WAS  
 $(V_{GS} - V_T) = 0.8$  V

Gate	$I_D$ ( $\mu\text{A}/\mu\text{m}$ )	$g_m$ (mS/mm)	$g_m/I_D$ ( $\text{V}^{-1}$ )	$R_i$ ( $\Omega\text{-}\mu\text{m}$ )
Metal	2700	4800	2	39

# Essential Physics

- Model devices with ballistic transport
- Velocity of carriers is finite
- Density of states
  - Large for Si semiconductor. Allows for  $q n_s(0) \approx C_{ox}(V_{GS} - V_T)$ ,
- In limit, scattering unlikely important

# Power Limit (Next Class)

## Zhirnov, Limits to Binary logic Switch Scaling

$$\Delta x \Delta p \geq \hbar$$

$$\Delta E \Delta t \geq \hbar.$$

$$\begin{aligned} x_{\min} &= \frac{\hbar}{\Delta p} \\ &= \frac{\hbar}{\sqrt{2m_e E_{\text{bit}}}} \\ &= \frac{\hbar}{\sqrt{2m_e k_B T \ln 2}} \\ &= 1.5 \text{ nm} \quad (T = 300 \text{ K}). \end{aligned}$$