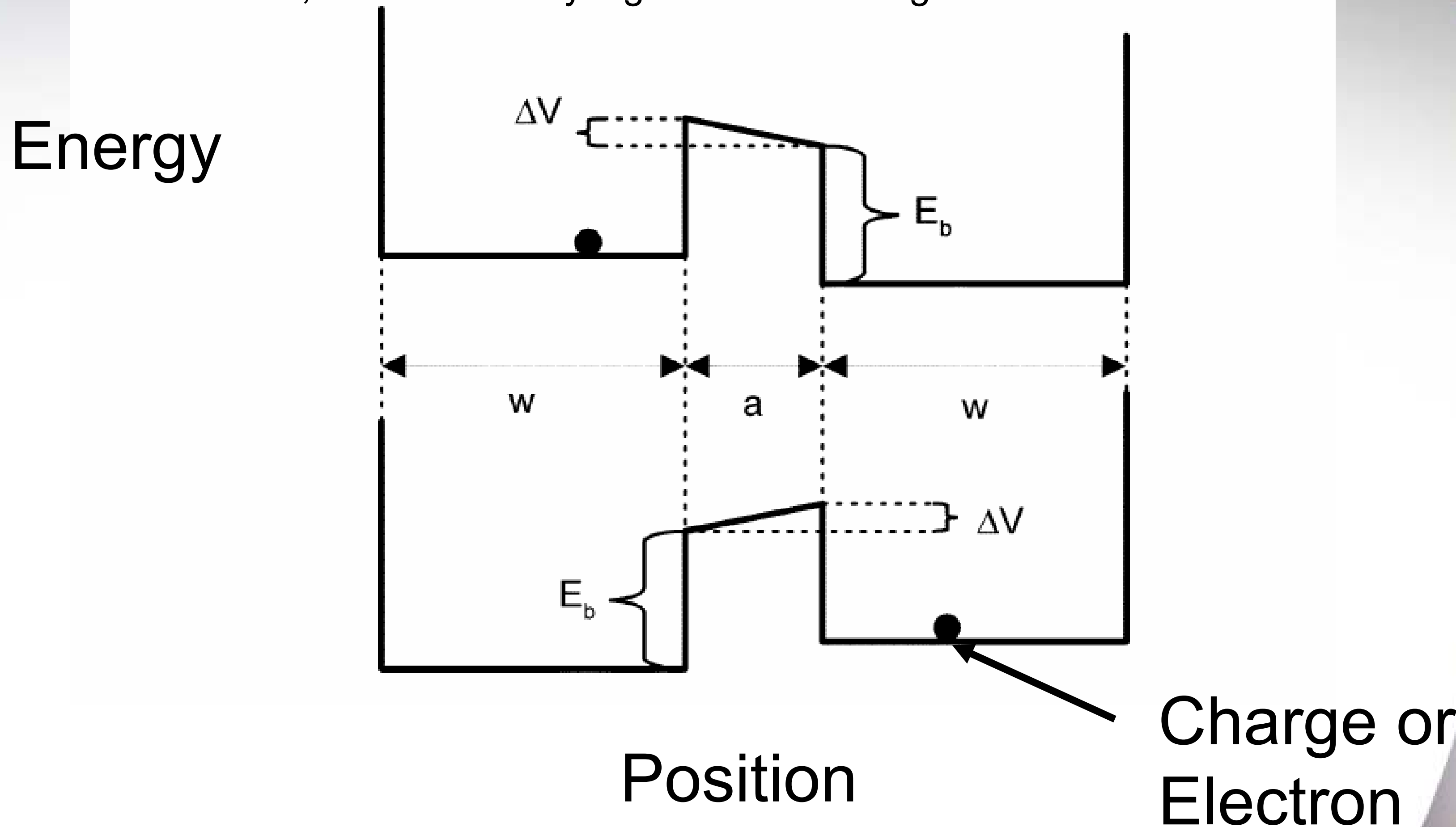
Lecture : 5
Limits for Si MOSFETs (Continued)

Last time: Simple Model for MOSFET

Zhirnov, Limits to Binary logic Switch Scaling

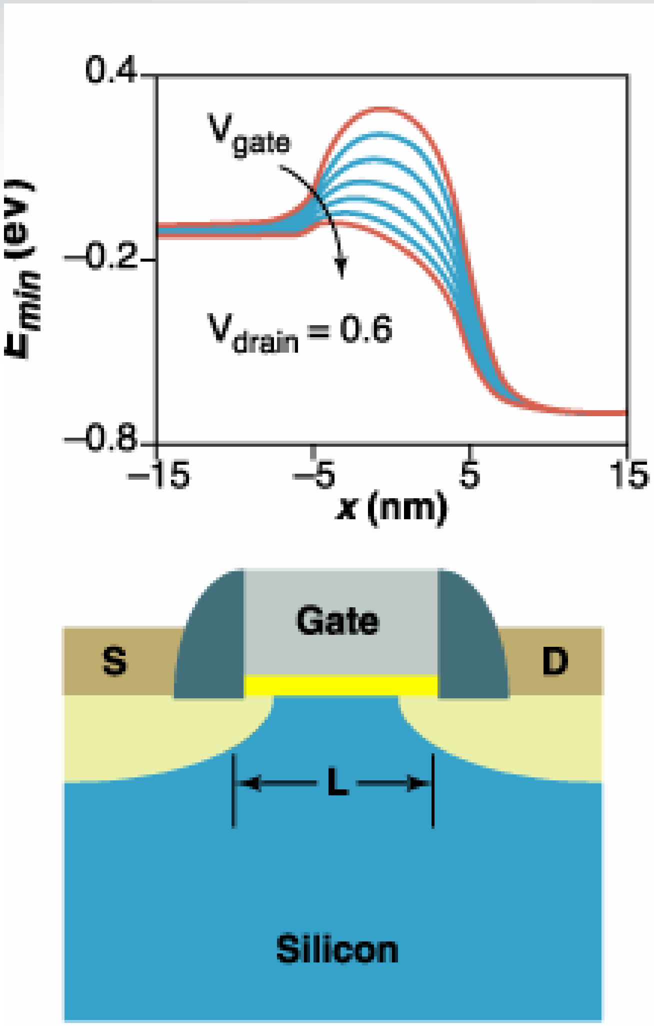


What are some requirements that information is not lost?

Summary of Questions I Was Asked During Office Hours

- How does the gate physically control the barrier
- How much does the barrier need to be lowered for current to flow
- What is Ballistic vs classical transport
- How does the Ballistic MOSFET Eq. compare to whats taught in Digital VLSI course
- Physical to electrical T_{OX} difference

How Does Gate Control Barrier



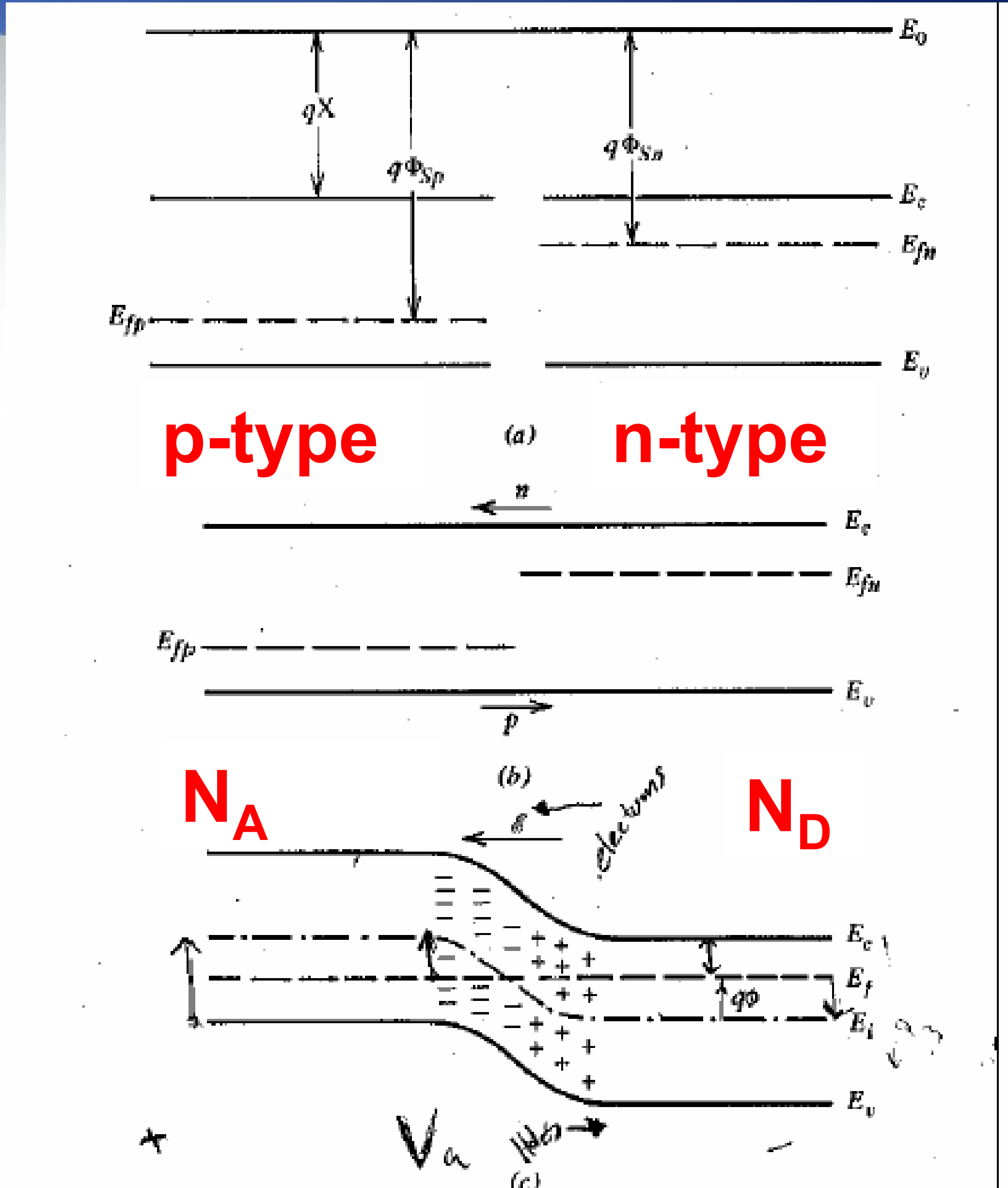
Simple principle “when the gate voltage is low, an energy barrier prevents electrons from flowing from source to drain, where as a high gate voltage lowers the energy barrier, allowing current to flow”

Mark Lundstrom

Science, Vol 299, Issue 5604, 210-211 , 10 January 2003

How is the Barrier Created?

- Build in potential barrier
- N and p type silicon
- In contact allowing diffusion



How is the Barrier Created?

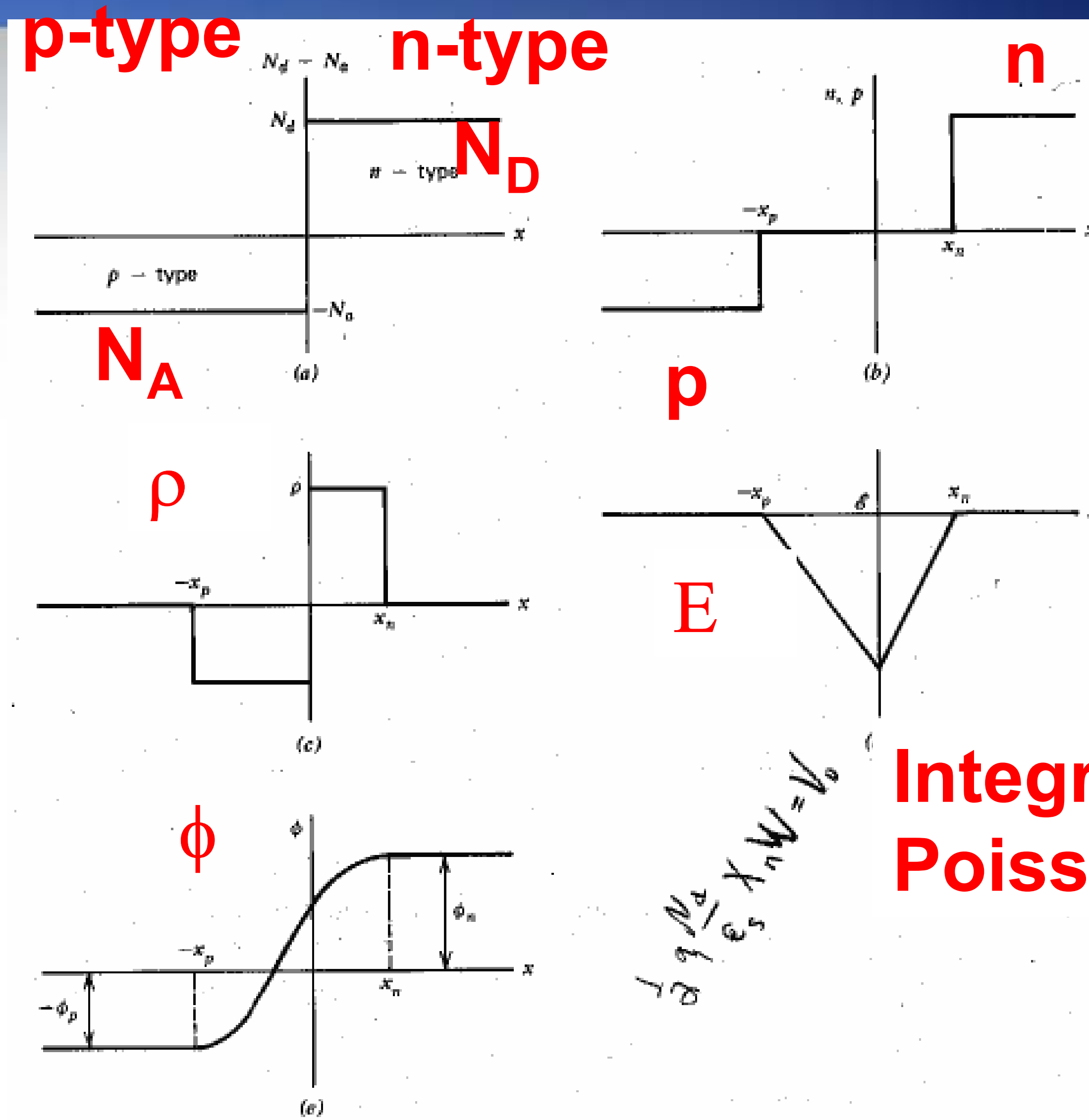
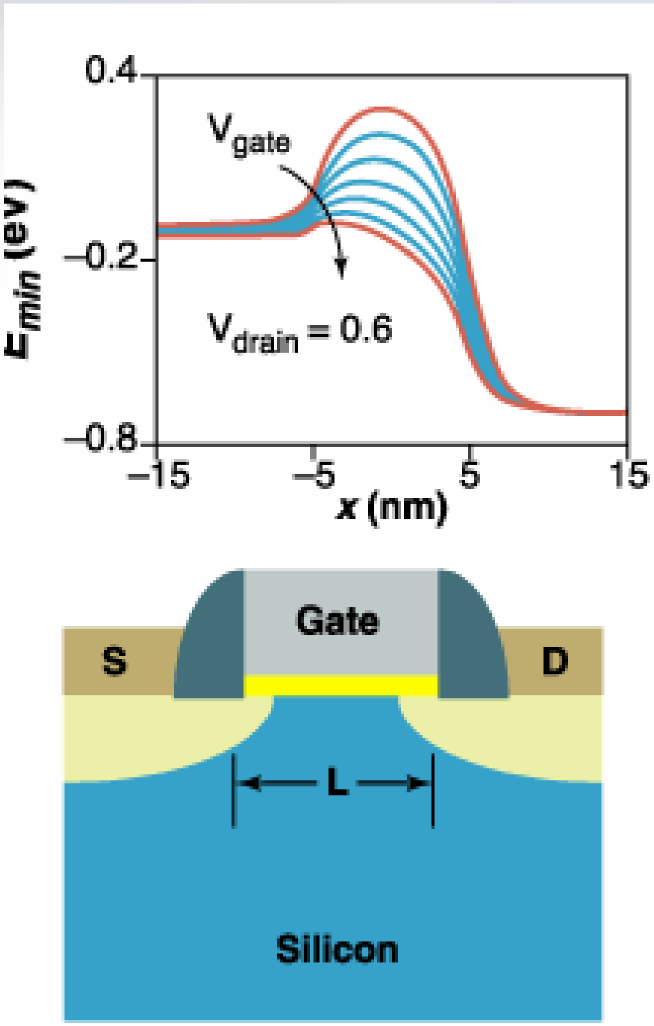


Figure 4.4 Properties of a step junction as functions of position using the complete-depletion approximation: (*a*) net dopant concentration, (*b*) carrer densities, (*c*) space charge used in Poisson's equation, (*d*) electric field found from first integration of Poisson's equation, and (*e*) potential obtained from second integration.

Muller and Kamins

How Does MOSFET Switch "on"



Ideally, switch "on" abruptly. BUT current is controlled by thermal emission over an energy barrier, it takes a change in gate voltage of at least 60mV to change the current by a factor of 10 at room temperature.

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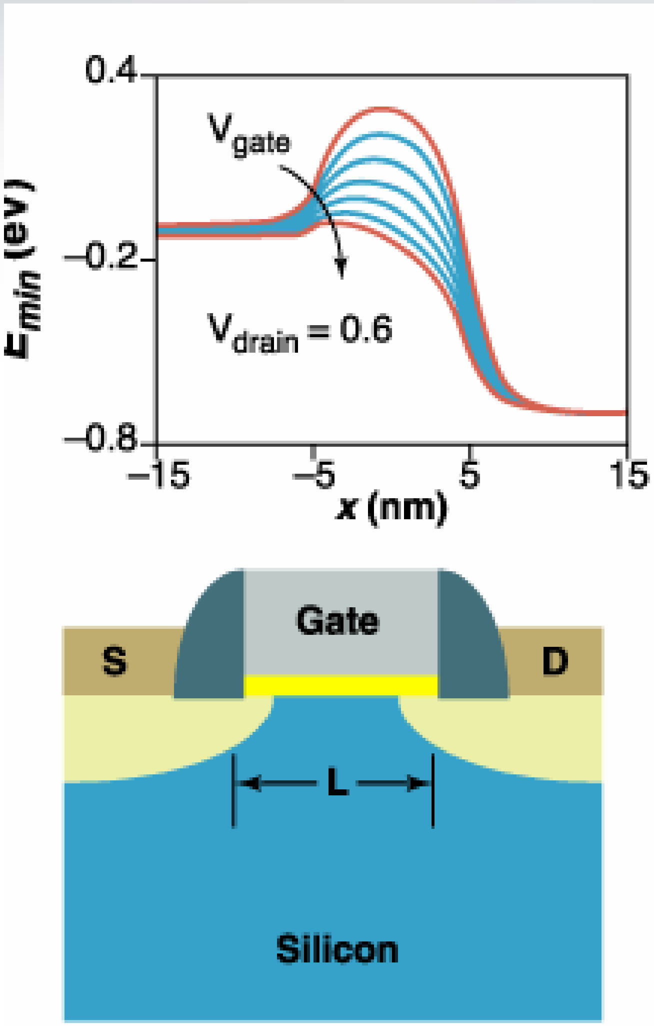
What is DIBL / Short channel effects (drain induced barrier lowering)



Ideally only gate controls the barrier height. For small MOSFETs, 2D electrostatics (.i.e the drain voltage) lower the barrier. Loss of gate control

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Ballistic vs Classical Transport

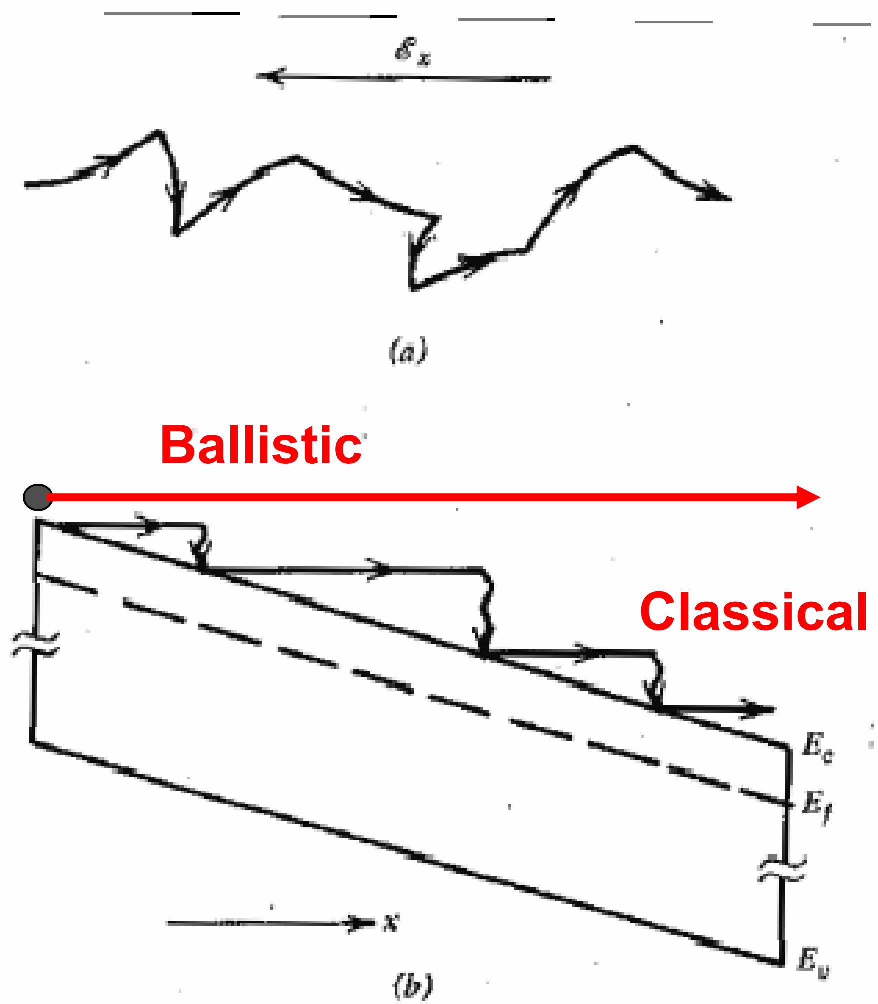


Figure 1.13 (*a*) The motion of an electron in a solid under the influence of an applied field. (*b*) Energy-band representation of the motion, indicating the loss of energy when the electron undergoes a collision.

Muller and Kamins

Ballistic Limit

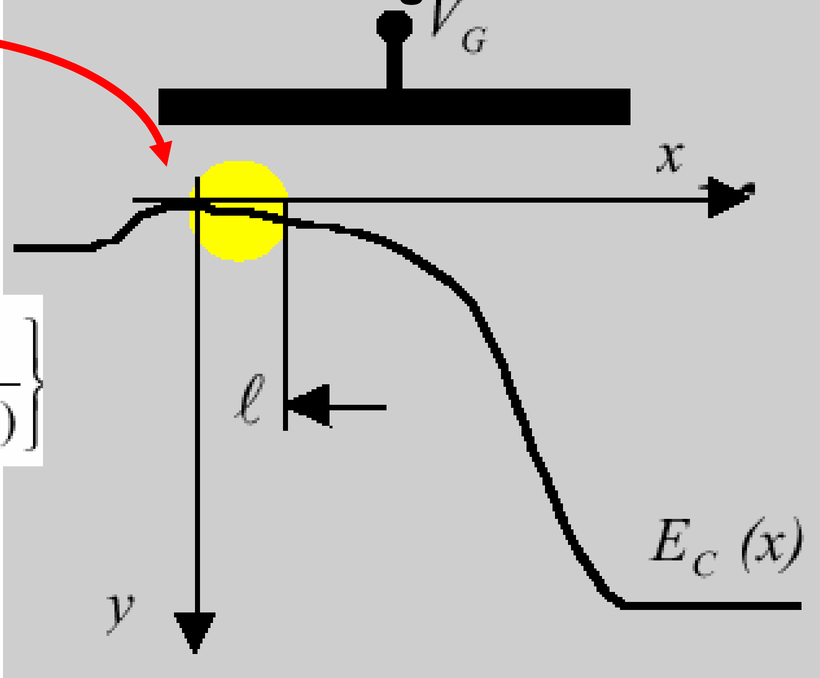
- Simple ballistic picture: The mean free path being much larger then channel length
- Ballistic limit corresponds to the channel length approaching zero
- No scattering before traveling distance ℓ which drops kT/q potential.
  – Scattering after dropping kT/q unlikely to emerge from the channel at source
- 0.35um devices operate at ~1/2 ballistic limit (IEDM Lundstrom)

Alternate MOSFET Description Equations

V_T = thermal velocity

r= backscattering coefficient

$$q\, n_s(0) \approx C_{ox}(V_{GS} - V_T),$$



$$I_D = W\, C_{ox} \langle \upsilon(0) \rangle (V_{GS} - V_T),$$

$$\langle \upsilon(0) \rangle = \left(\frac{1-r}{1+r} \right) \upsilon_T \qquad \upsilon_T = \sqrt{\frac{2 k_B T_L}{\pi m_t^*}} \left\{ \frac{\mathscr{F}_{1/2}(\eta)}{\ell n(1+e^{\eta})} \right\}$$

$$I_D = W\, C_{ox} \sqrt{\frac{2 k_B T_L}{\pi m_t^*}} \cdot (V_{GS} - V_T),$$

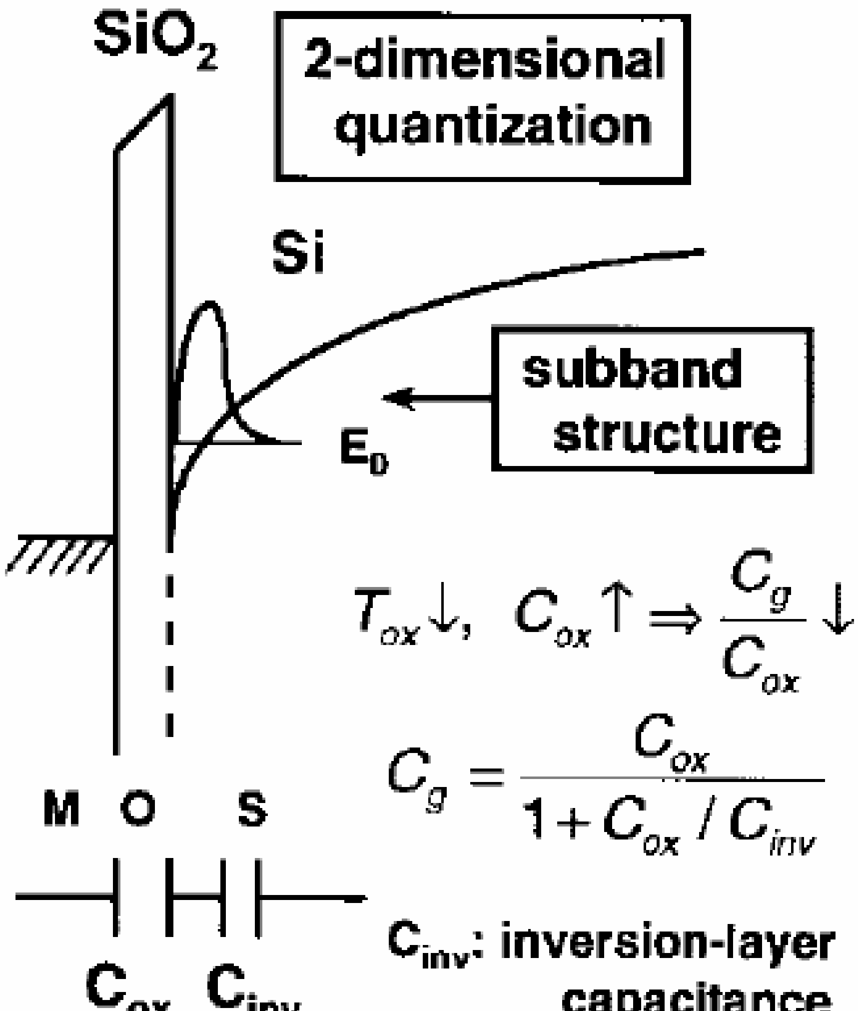
vs. classical expression

$$\boxed{I_D = \mu \cdot C_{OX} \cdot \frac{W}{L} \cdot \frac{(V_{GS} - V_T)^2}{2}, \text{ for } V_{DS} \geq (V_{GS} - V_T)}$$

Lundstrom, Essential Physics of Carrier Transport in Nanoscale MOSFETs

Physical vs Electrical T_{ox}

Takagi, Characterization of inversion layer capacitance of holes in Si MOSFETS



$$T_{ox}\downarrow,\ C_{ox}\uparrow \Rightarrow \frac{C_g}{C_{ox}}\downarrow$$

$$C_g = \frac{C_{ox}}{1 + C_{ox}/C_{inv}}$$

Last time: Evaluated Max ID

V_T = thermal velocity

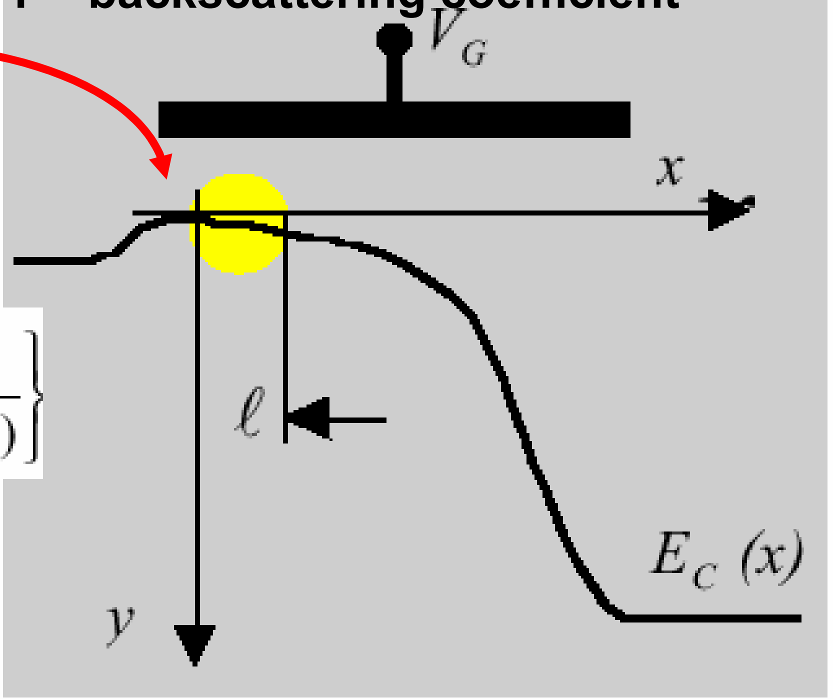
r= backscattering coefficient

$$q\,n_s(0) \approx C_{ox}(V_{GS} - V_T),$$

$$I_D = W\,C_{ox}\langle \upsilon(0)\rangle (V_{GS} - V_T),$$

$$\langle \upsilon(0)\rangle = \left(\frac{1-r}{1+r}\right)\upsilon_T \qquad \upsilon_T = \sqrt{\frac{2k_BT_L}{\pi m_t^*}}\left\{\frac{\mathcal{F}_{1/2}(\eta)}{\ell n(1+e^{\eta})}\right\}$$

$$I_D = W\,C_{ox}\sqrt{\frac{2k_BT_L}{\pi m_t^*}}\cdot(V_{GS} - V_T),$$



Example on board last time :

I_D ~2.0mA/um = 2000uA/um

Results in Paper

Production today

ID= 1250

Intel 65nm 2004 IEDM paper?

ID= 1450

TABLE I
COMPUTED PERFORMANCE OF THE MODEL BALLISTIC DEVICE AT 300K. THE THRESHOLD VOLTAGE WAS —0.4 V, THE GATE OVERDRIVE WAS $(V_{GS} - V_T) = 0.8$ V, AND THE DRAIN VOLTAGE WAS 1.0 V

Gate	I_D (µA/µm)	g_m (mS/mm)	g_m/I_D (V^{-1})	R_i (Ω-µm)
Metal	2200	3500	1.7	44
Polysilicon	1700	2800	1.7	52

TABLE II
COMPUTED PERFORMANCE OF THE MODEL BALLISTIC DEVICE AT 77K. THE THRESHOLD VOLTAGE WAS —0.5 V AND THE GATE OVERDRIVE WAS $(V_{GS} - V_T) = 0.8$ V

Gate	I_D (µA/µm)	g_m (mS/mm)	g_m/I_D (V^{-1})	R_i (Ω-µm)
Metal	2700	4800	2	39

MOSFET Size LimitToday: A Quantum Mechanical Estimate

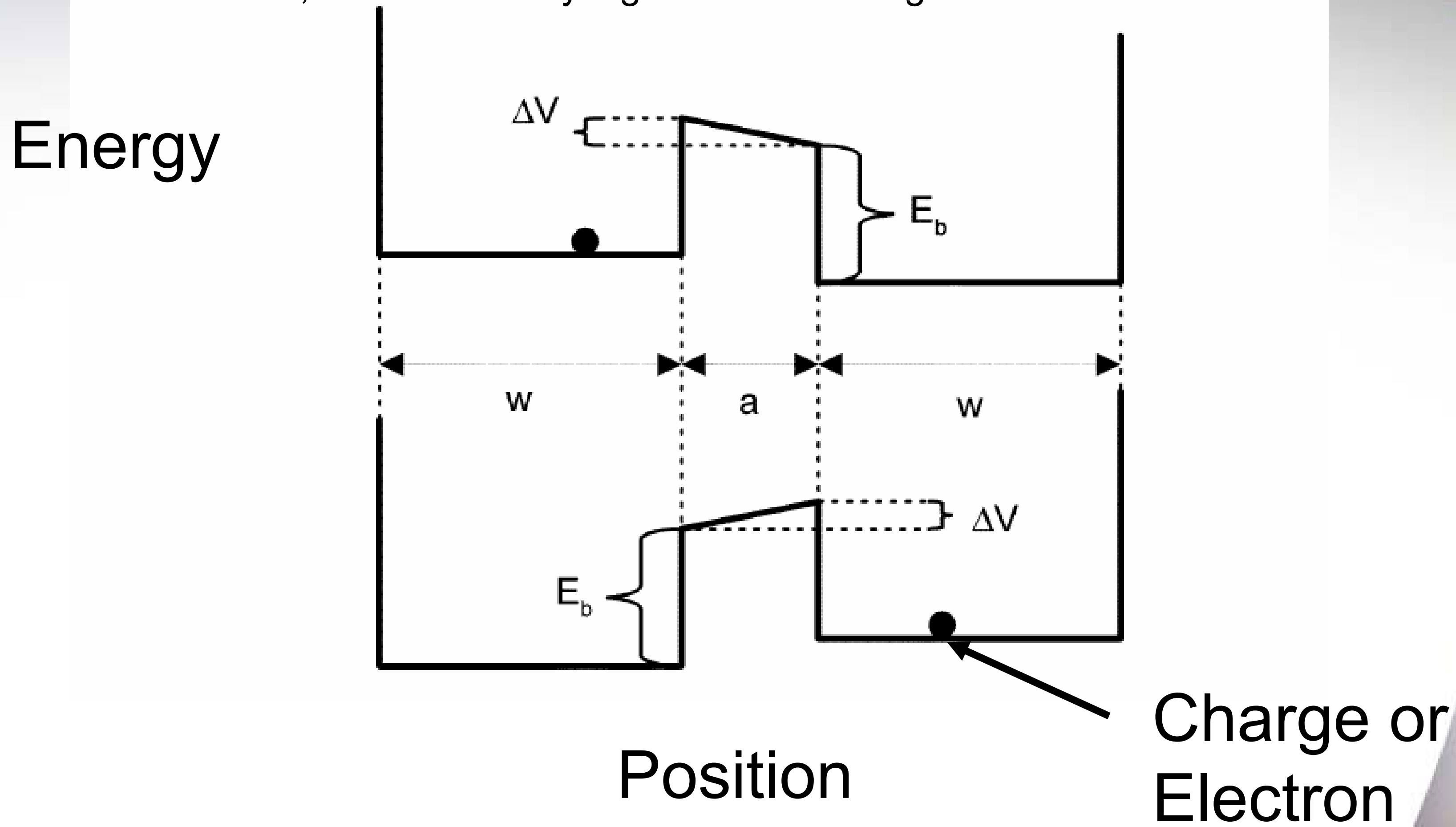
Limits to Binary Logic Switch Scaling—A Gedanken Model

VICTOR V. ZHIRNOV, RALPH K. CAVIN, III, FELLOW, IEEE,
JAMES A. HUTCHBY, SENIOR MEMBER, IEEE, AND GEORGE I. BOURIANOFF, MEMBER, IEEE

Invited Paper

Again, Simple Model for MOSFET

Zhirnov, Limits to Binary logic Switch Scaling



Many factors limit MOSFET size: tunneling, drain contolling barrier

Quantum Limit

Zhirnov, Limits to Binary logic Switch Scaling

$$\Delta x \Delta p \geq \hbar$$
$$\Delta E \Delta t \geq \hbar.$$

$$\begin{aligned} x_{\min} &= \frac{\hbar}{\Delta p} \\ &= \frac{\hbar}{\sqrt{2 m_e E_{\mathrm{bit}}}} \\ &= \frac{\hbar}{\sqrt{2 m_e k_B T \ln 2}} \\ &= 1.5\ \mathrm{nm} \quad (T = 300\ \mathrm{K}). \end{aligned}$$

Quantum mechanic allows for a very small switch. Other factors materials limits / transistors electro-statics WILL limit before this.