

# Lecture : 7

## Limits for Si MOSFETs

# Other MOSFET LIMITS

- Performance limit (last time)
- Size limit (last time)
  - Estimate based on quantum principles (this lecture)
- Device and Material Limits (this time)
  - Minimum  $L_{\text{GATE}}$  based on short channel effects
  - Minimum  $L_{\text{GATE}}$  based on S/D tunneling
- In general how one should look at a new device
  - Performance limit
  - $L_{\text{GATE}}$  minimum typically based on SCE or S/D tunneling

# References

CMOS design  
near the limit  
of scaling

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by Y. Taur

## Investigation of Performance Limits of Germanium Double-Gated MOSFETs

Tony Low<sup>1</sup>, Y. T. Hou<sup>1</sup>, M. F. Li<sup>1,2</sup>, Chunxiang Zhu<sup>1</sup>, Albert Chin<sup>3</sup>, G. Samudra<sup>1</sup>, L. Chan<sup>4</sup> and D. -L. Kwong<sup>5</sup>

## Does source-to-drain tunneling limit the ultimate scaling of MOSFETs?

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## Fundamental Limits of Silicon Technology

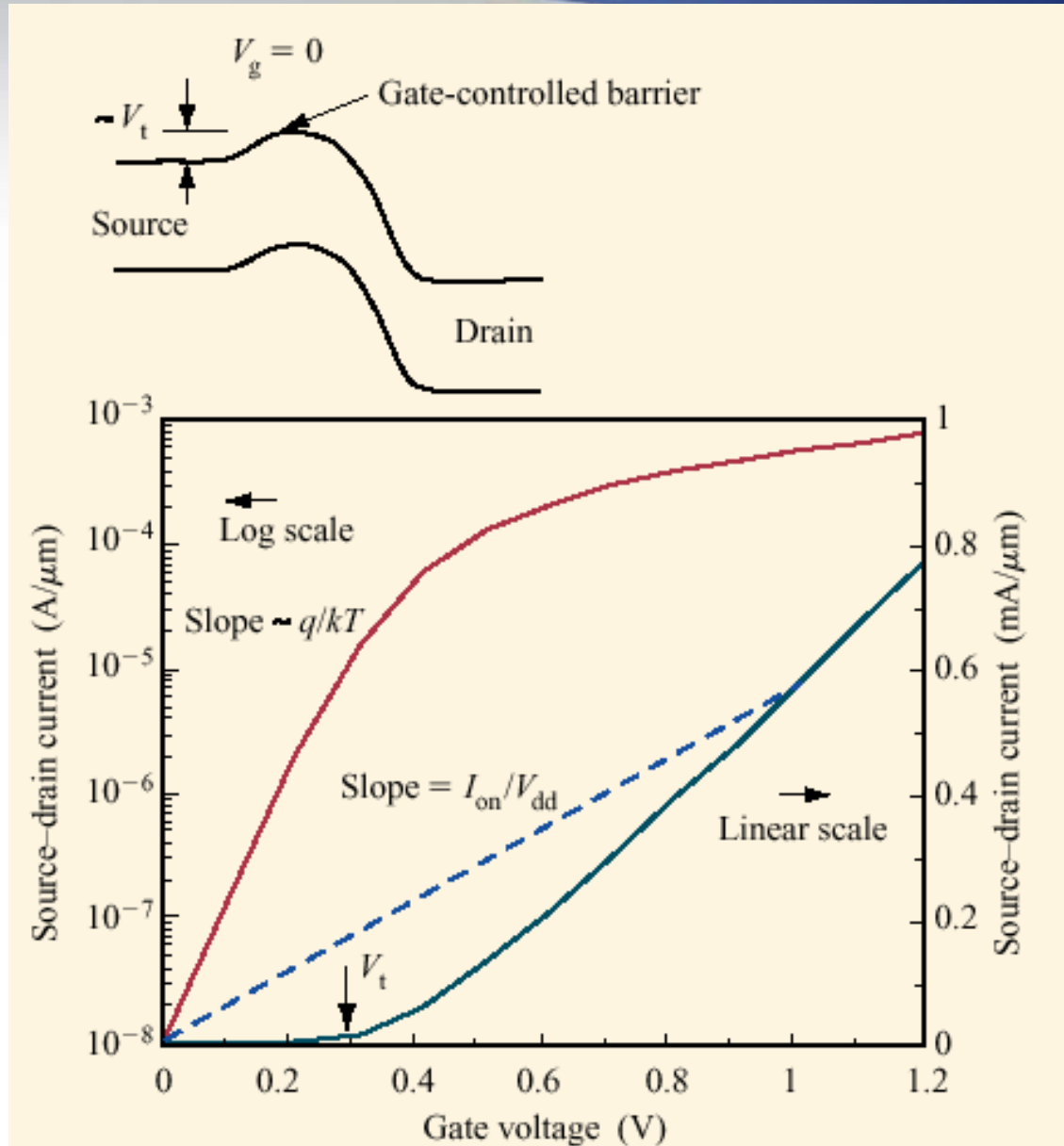
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ROBERT W. KEYES, FELLOW, IEEE

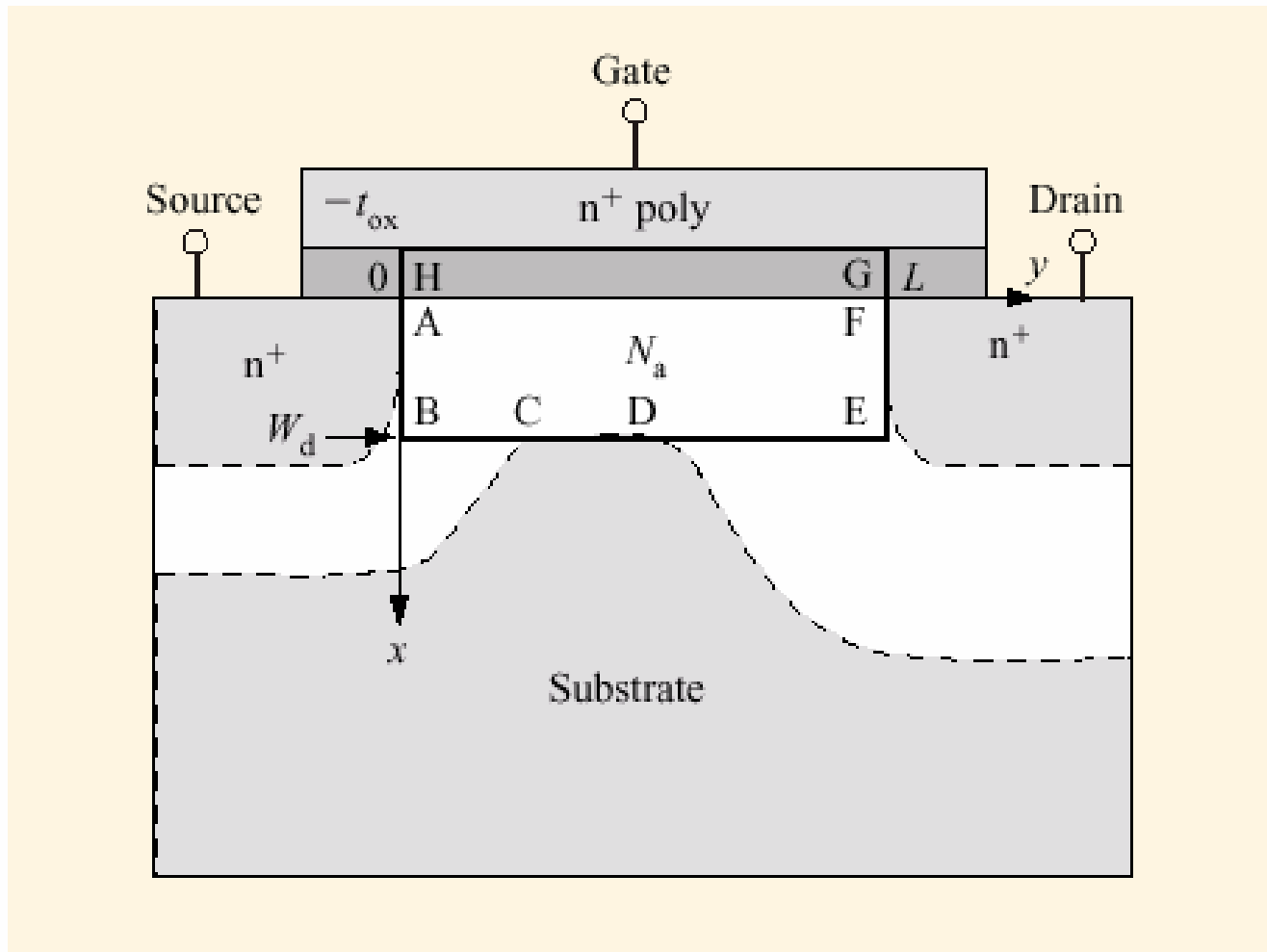
# Again What Limit Minimum $L_{\text{GATE}}$ : High $I_{\text{OFF}}$ (Not a Good Switch)

Leakage over or through the barrier

Taur, CMOS design near the limit of scaling



# Planar MOSFET and Short Channel Effects



Taur, CMOS design near the limit of scaling

S. E. Thompson EEL 6935

# Minimum $T_{OX}$ Sets Minimum $L_{GATE}$

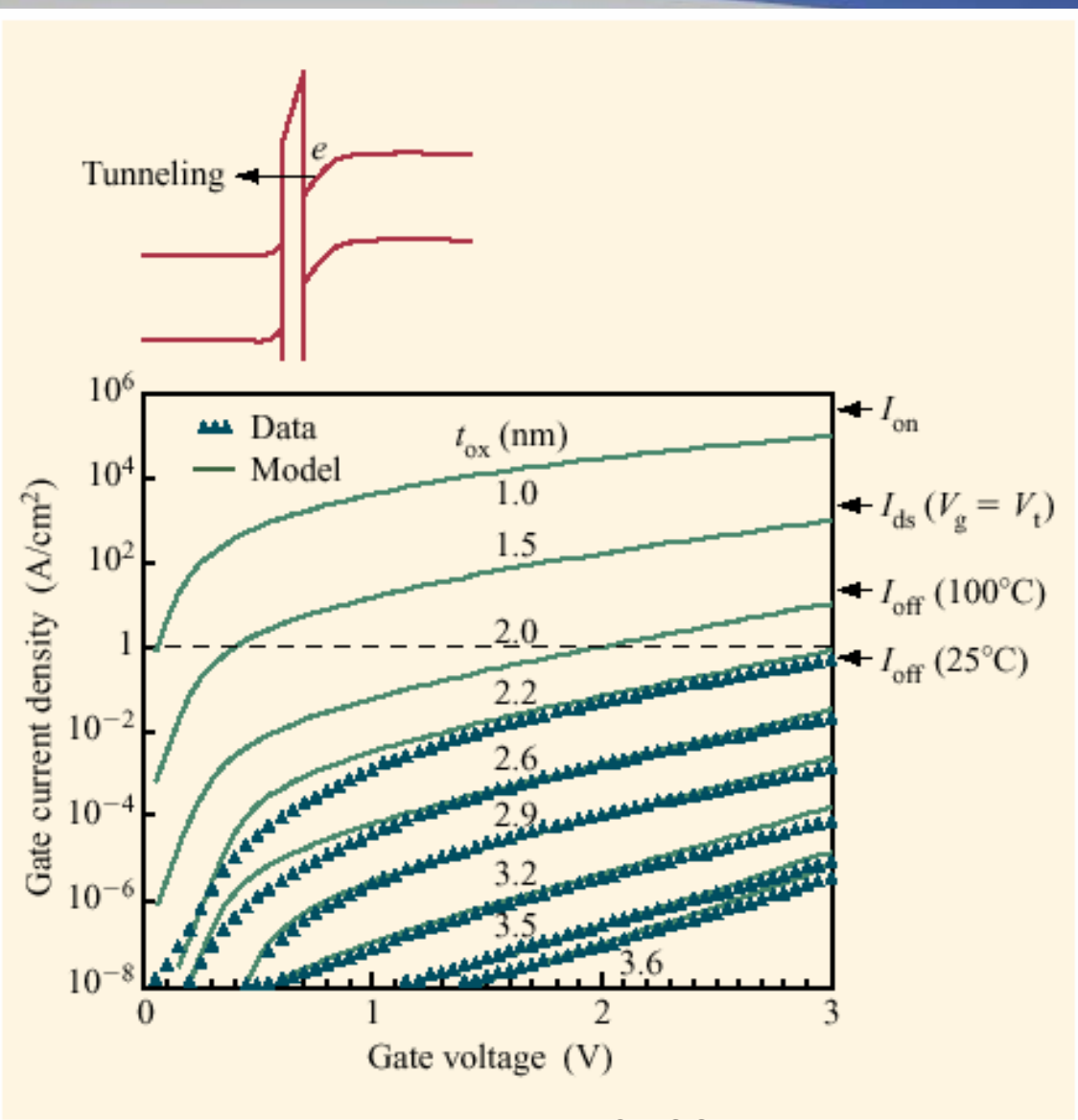
$$S = m(\ln 10) \frac{kT}{q} = \left( 1 + \frac{\epsilon_{si} t_{ox}}{\epsilon_{ox} W_{dm}} \right) (\ln 10) \frac{kT}{q},$$

A reasonable upper limit is  $t_{ox}/W_{dm} = 0.1$ , or

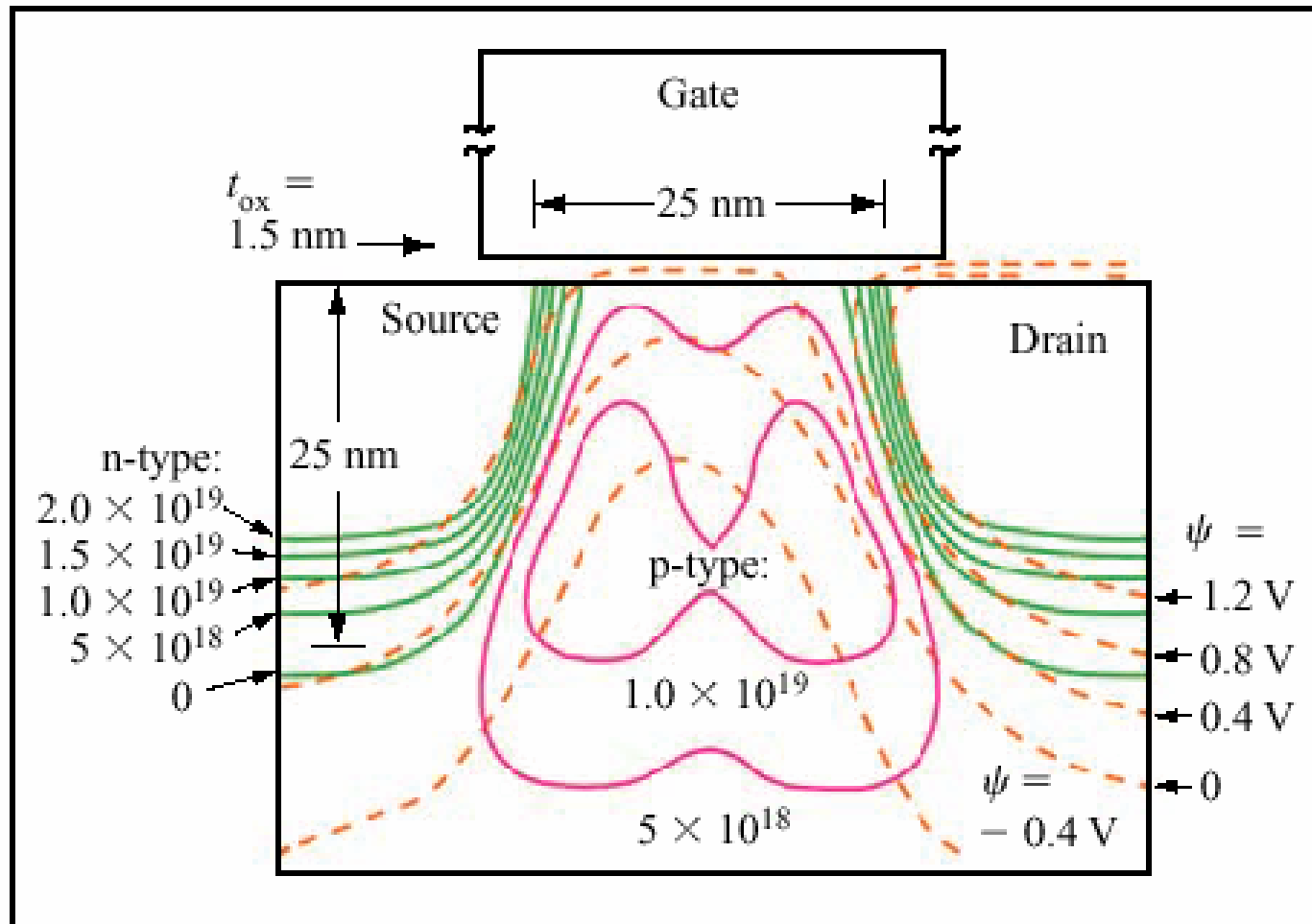
$$L_{GATE} = 20 T_{OX}$$

Taur, CMOS design near the limit of scaling

# Oxide Thickness Set Depletion Width .....Minimum Oxide Thickness

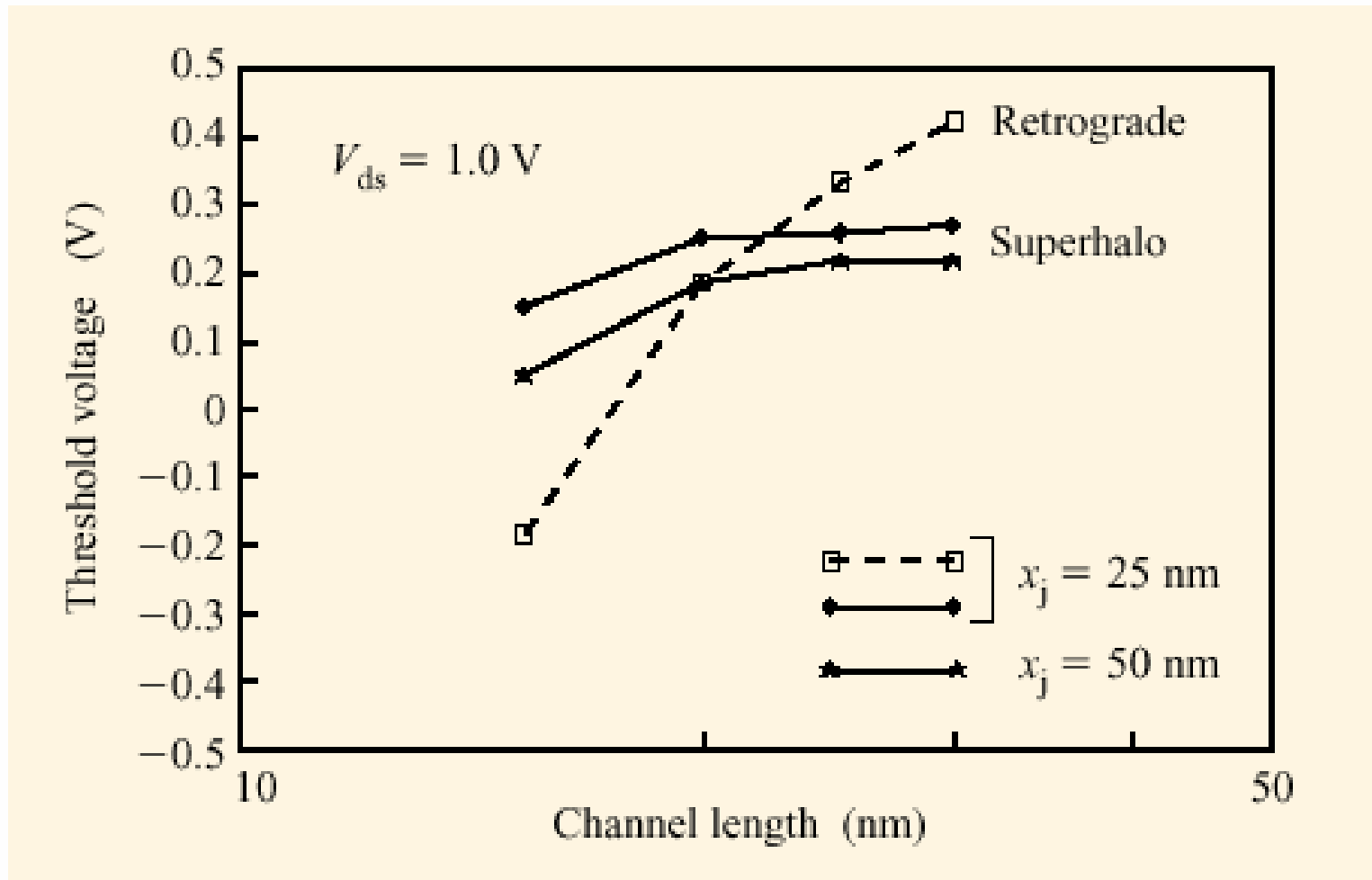


# Minimum $L_{\text{GATE}}$ for Planar CMOS $\sim 25$ nm (Is 15? 20? Planar CMOS possible?)



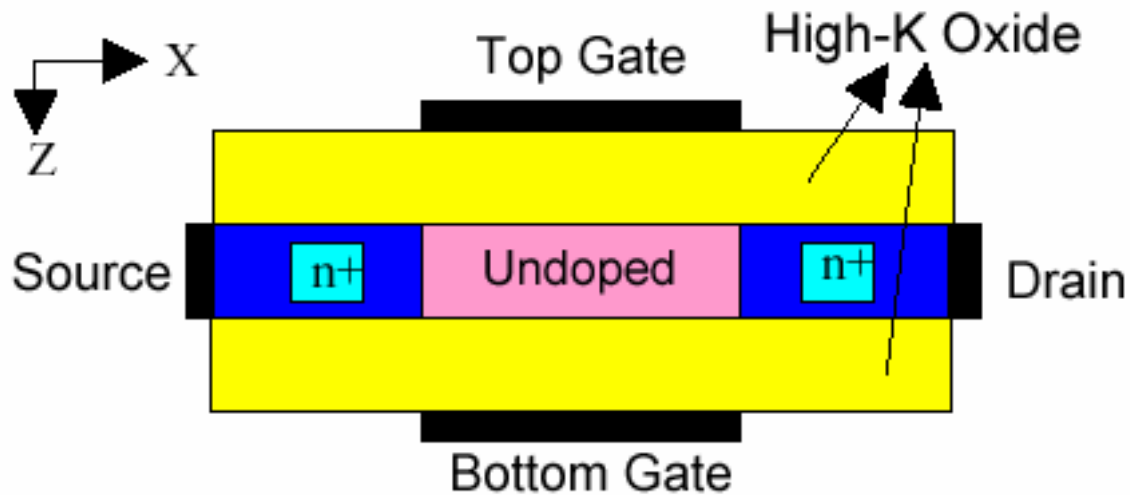
Taur, CMOS design near the limit of scaling

# What happens if $L_{\text{GATE}} = 20 T_{\text{OX}}$ ?



Taur, CMOS design near the limit of scaling

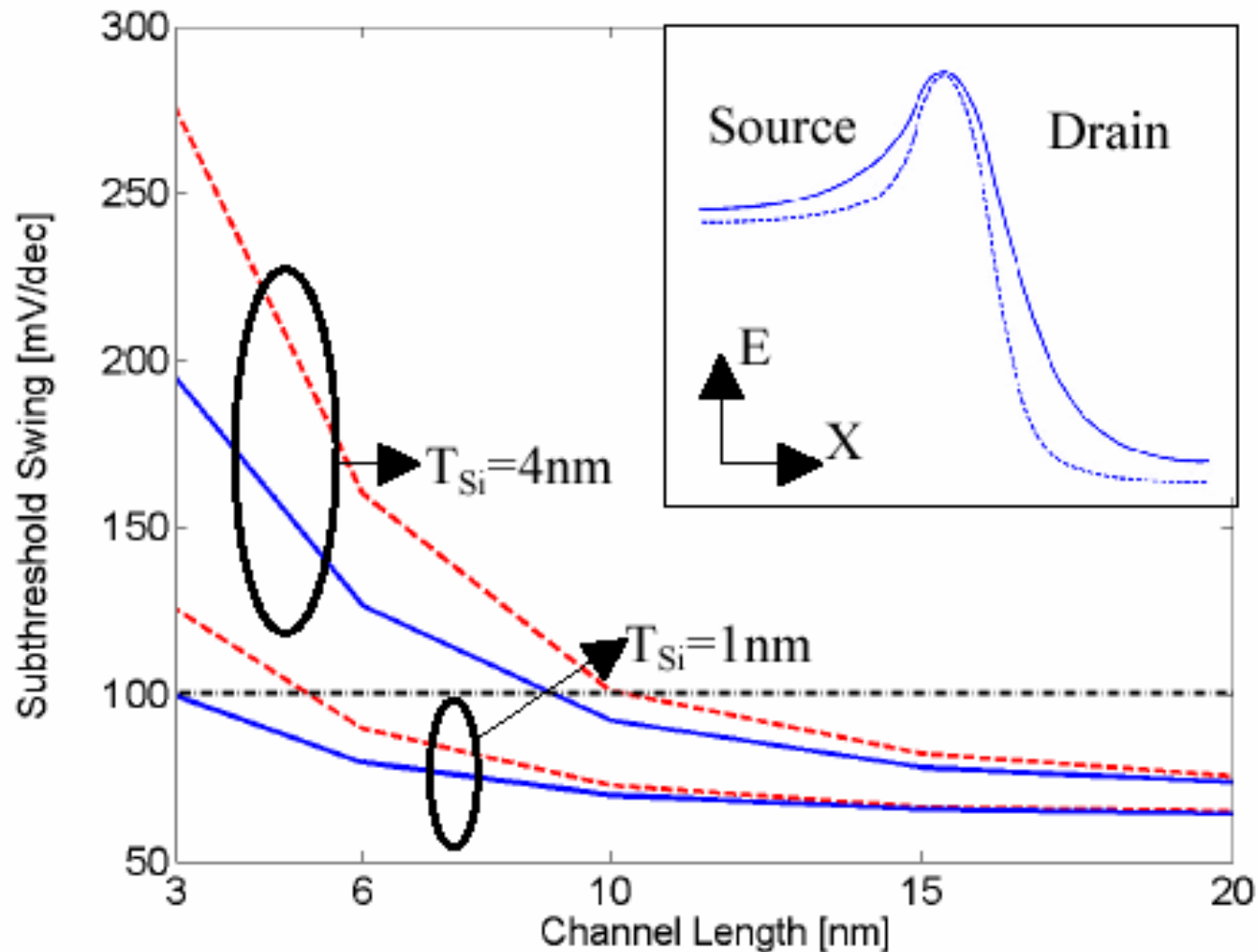
# Change Device Structure to 2 Gates Improves SCE



Lundstrom: Does source-to-drain tunneling limit the ultimate scaling of MOSFETs

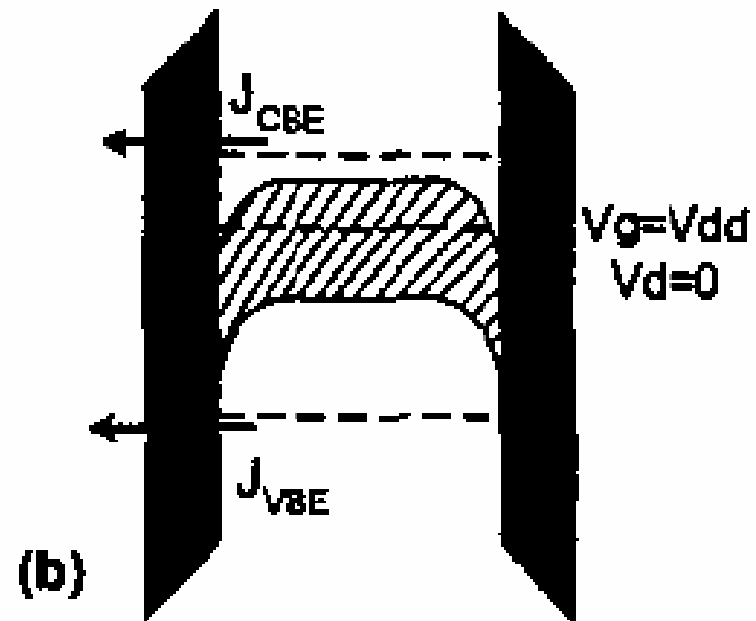
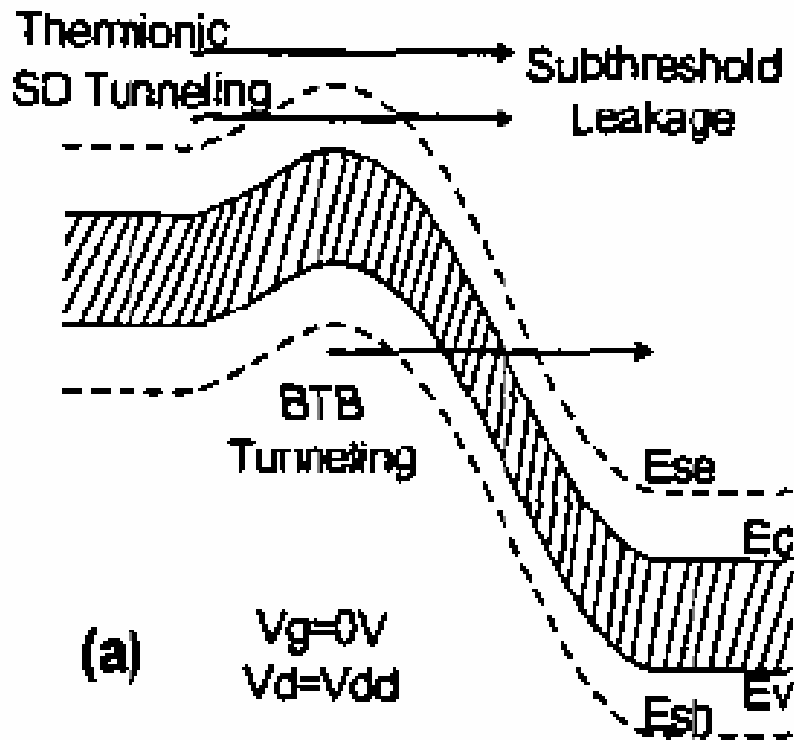
# 5-10nm Double Gate MOSFETs Possible

## Does industry move to these devices?

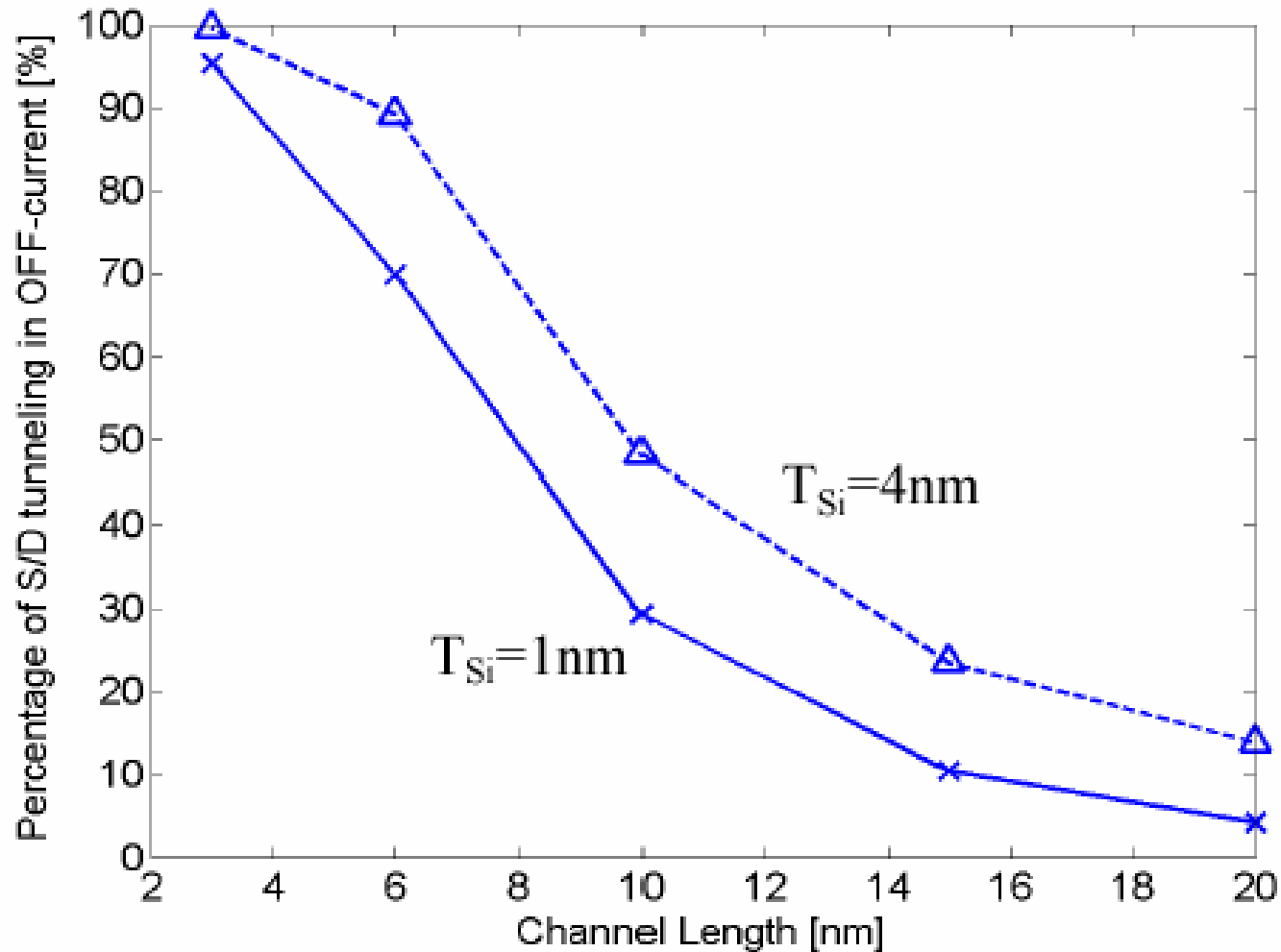


Lundstrom: Does source-to-drain tunneling limit the ultimate scaling of MOSFETs

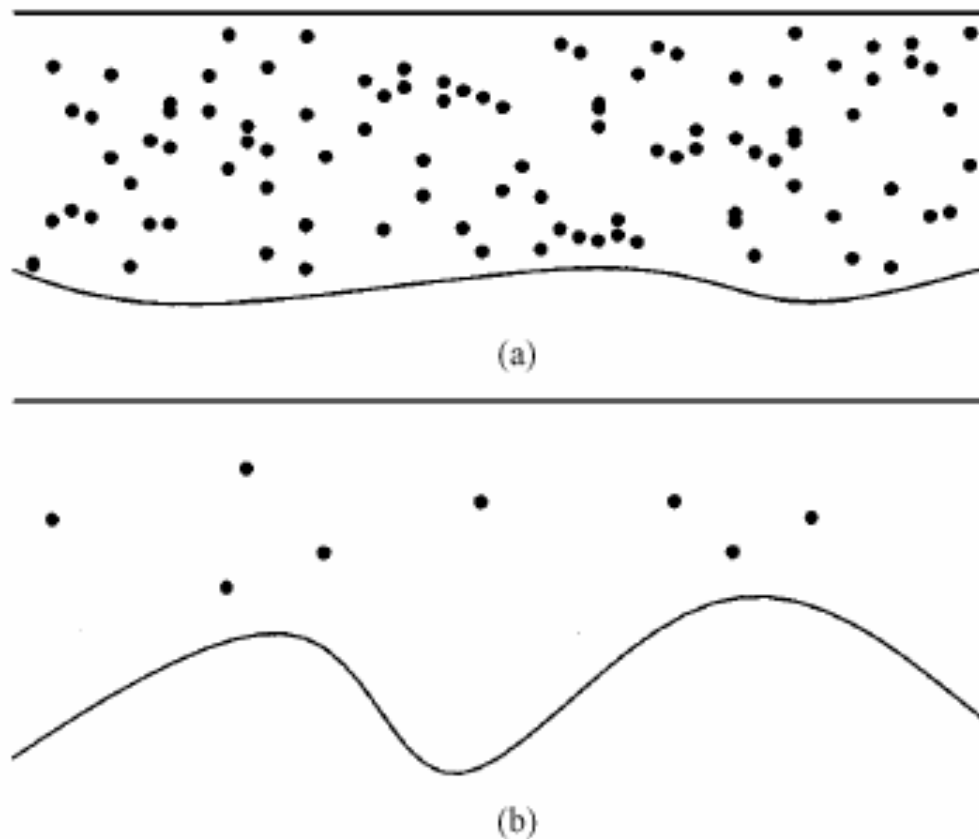
# Other Limits: Source to Drain Tunneling



# Limits devices at ~ 10nm



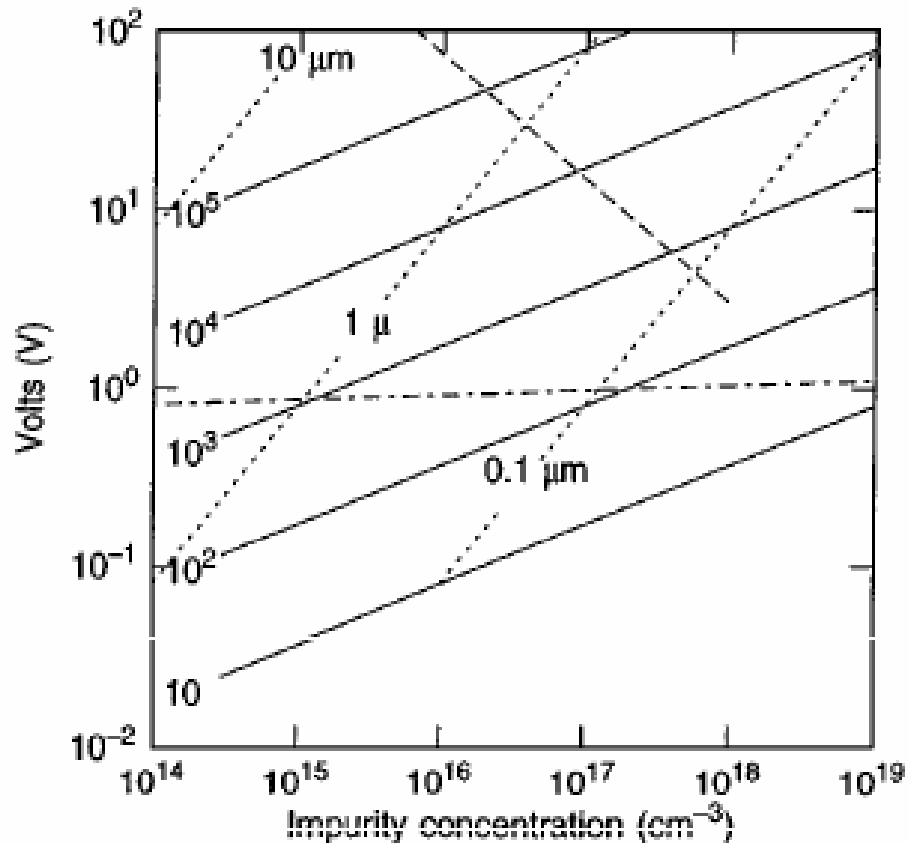
# Other limits: Dopant fluctuations



**Fig. 3.** Effect of small numbers of charged impurities on the form of the depleted layer in a pn junction. (a) Number of dopant atoms per cube is large and (b) approaching one.

# # Finite # of Dopant Atoms

## Why is this an issue?



Keys, Fundamental Limits of Silicon Technology

# Summary

- Device SCE limits the planar MOSFET at  $\sim 25\text{nm}$ .
  - Much larger  $L_{\text{GATE}}$  limit than any quantum limits
- But limit is only for a planar MOSFET and does not consider high k gates.
- Multi gates MOSFETs
  - Changes SCE relationship and allows for  $< 10\text{nm}$  devices
- At  $10\text{nm}$  direct source-to-drain tunneling limits present
- Limit for a Si charge controlled device is thus  $\sim 10\text{nm}$