Measurement of conduction band deformation potential constants using gate direct tunneling current in *n*-type metal oxide semiconductor field effect transistors under mechanical stress

Ji-Song Lim, Xiaodong Yang, Toshikazu Nishida, and Scott E. Thompson[a)]
Department of Electrical and Computer Engineering, University of Florida, Gainesville, Florida 32611

(Received 20 March 2006; accepted 13 June 2006; published online 17 August 2006)

An experimental method to determine both the hydrostatic and shear deformation potential constants is introduced. The technique is based on the change in the gate tunneling currents of Si-metal oxide semiconductor field effect transistors (MOSFETs) under externally applied mechanical stress and has been applied to industrial *n*-type MOSFETs. The conduction band hydrostatic and shear deformation potential constants (Ξ_d and Ξ_u) are extracted to be 1.0 ± 0.1 and 9.6 ± 1.0 eV, respectively, which is consistent with recent theoretical works. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2245373]

In the design of strained silicon devices which are now standard in sub-90 nm production technologies,[1–4] it is essential to accurately quantify strain-induced energy level shifts and splitting which are modeled by deformation potentials. Strain-induced band splitting removes conduction and valence band degeneracies and is primarily responsible for the engineered mobility enhancement.[1–4] Strain-induced shifts in the energy levels alter the electron affinity which shifts the metal-oxide-semiconductor field-effect transistor (MOSFET) threshold voltage. While the shear deformation potentials used to calculate energy level splitting are well known with good accuracy from piezoresistance measurements (Ξ_u=9.16 eV),[5] the hydrostatic deformation potential is difficult to directly measure using the conventional optical techniques. As a result, a very wide range of values including opposite signs have been reported (1.13 to −10.7 eV).[6] This results since optical experimental techniques directly measure differences in energy levels (for example, strain-induced band gap narrowing) but not the absolute position of the energy levels which leaves large uncertainty in important band parameters such as the electron affinity of strained Si.[7] Recently, numerical calculations by Fischetti and Laux[8] have helped resolve some of the uncertainties with the hydrostatic deformation potential and suggest a value of Ξ_d=1.1 eV. In this letter, we present a method to extract both the shear and hydrostatic deformation potentials using the strain and gate voltage dependence of the gate tunneling current.

A four-point bending jig applies compressive mechanical stress longitudinal to the ⟨110⟩ channel on (100) *n*-type MOSFET (*n*-MOSFET) samples.[9] The MOSFETs consist of arsenic doped n^+ polycrystalline Si gate on top of 1.3 nm nitrided SiO_2 gate dielectric on 10^{17} cm^{-3} boron doped *p* well. The gate tunneling current is measured with the drain, source, and body all tied to ground and the gate positively biased on 2 and 4 μm *n*-MOSFET samples using a Keithley 4200 dc characterization system. It has previously been reported that stress alters the gate tunneling currents on both (100) *n*- and *p*-type MOSFETs,[10] with tensile stress typically used for *n*-MOSFET. In this work, we apply compressive stress since electrons primarily populate only the two lowest energy levels under this condition[11] [population of Δ_2 valley next lowest subband, $E'_{\Delta_2}(\sigma)$, is negligible which simplifies the interpretation of the tunneling current data]. A schematic drawing of the direct tunneling process from the Δ_2 and Δ_4 subbands and the effect of stress on the subband energies are shown in Fig. 1. Stress alters the tunneling current in two ways: (1) Stress-induced energy level splitting causes a repopulation between Δ_2 and Δ_4. The lifetime of Δ_2 is significantly longer compared to Δ_4 due to the high out-of-plane mass ($0.92m_o$ vs $0.19m_o$). (2) The shift in the energy levels alters the SiO_2/Si barrier height. The change in the gate current versus applied compressive stress for different gate voltages is shown in Fig. 2(a). We observe the change normalized to zero stress, $[\Delta I_G(\sigma)/I_G(0)]$, is positive (increases) and is larger at low gate voltage. At high gate voltage, the change is a weak function of voltage. Both of these trends can be understood from how the vertical electric field and compressive stress shift and split the energy levels. At high gate voltage (high vertical field), Δ_2 is many kT below Δ_4 resulting in electrons primarily populating Δ_2. Hence at high gate voltage, a smaller change in the gate leakage results since compressive stress only alters the gate current by lowering the SiO_2/Si barrier height (shifting Δ_2 to higher energy as seen in Fig. 1). For low gate voltage, electrons populate both Δ_2 and Δ_4, so in addition to the stress-induced change in barrier height, stress also increases the population of electrons in Δ_4 which further increases the tunneling current (due

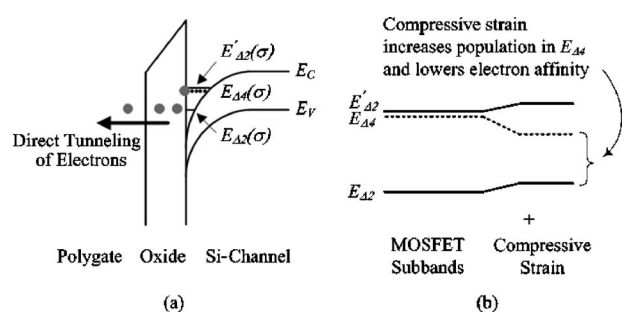

FIG. 1. (a) Schematic band diagram for the gate direct tunnel current in an *n*-MOSFET on a (100) wafer. (b) Δ_2 and Δ_4 energy level shifts under compressive stress and MOSFET inversion layer confinement. Under compressive stress, Δ_2 energy levels are raised while Δ_4 energy level (dotted line) is lowered.

[a)]Electronic mail: thompson@ece.ufl.edu

 © 2006 American Institute of Physics
Downloaded 11 Jan 2007 to 128.227.127.198. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp

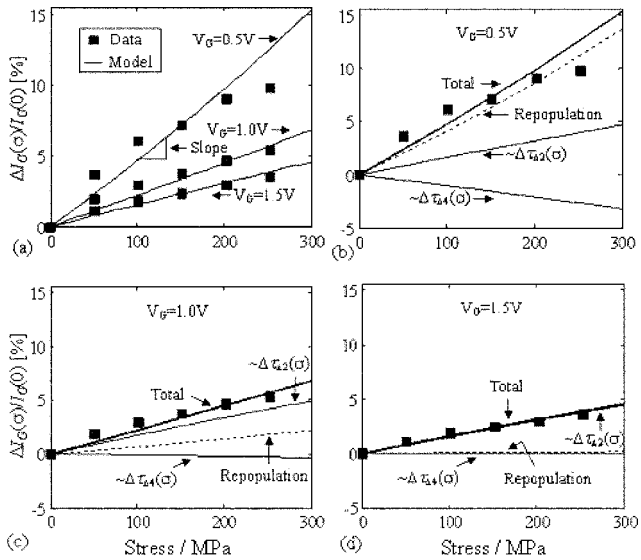

FIG. 2. (a) Relative direct tunnel current change $[\Delta I_G(\sigma)/I_G(0)]$ vs applied compressive stress at different gate voltages. Data (squares) were measured on industrial MOSFETs. The solid lines are our model. [(b)–(d)] Breakout of the various contributions to $\Delta I_G(\sigma)/I_G(0)$ at different gate voltages: [electron repopulation from Δ_2 to Δ_4 (dominates at low V_G), change in lifetime of Δ_2 or Δ_4 electrons due to change in barrier height].

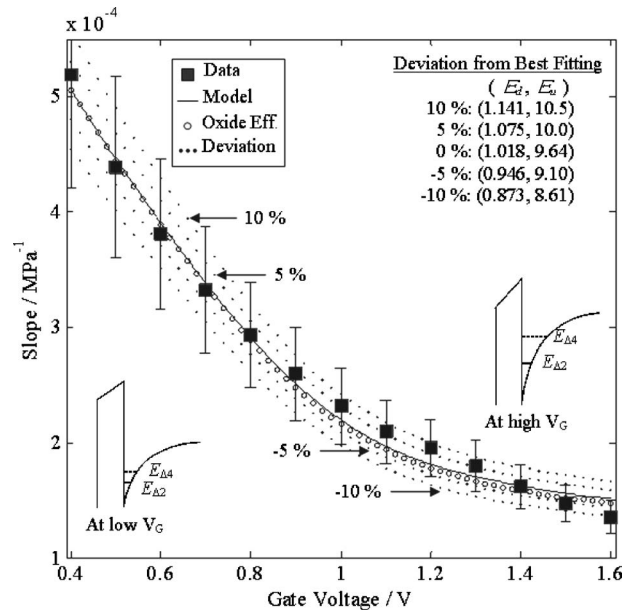

FIG. 3. Change in slopes $(d[\Delta I_G(\sigma)/I_G(0)]/d\sigma)$ vs gate voltage with 95% confidence error bars. Best fit for the entire data set occurs for Ξ_d and Ξ_u of 1.0 and 9.6 eV. Deviations from the best fitting values are shown by changing the deformation potentials by ~10%. The insets represent schematic band diagrams at low and high gate biases. Higher slopes at low V_G are due to a larger strain-induced repopulation between Δ_2 and Δ_4 subbands since their energy levels are closer to each other.

to the shorter lifetime in Δ_4 than Δ_2). Capturing the change in tunneling current with stress (or slope of curves in Fig. 2) for the full range of gate voltage, Fig. 3 shows the change in $d[\Delta I_G(\sigma)/I_G(0)]/d\sigma$ versus applied gate voltages. The slope was extracted from the raw data of $I_G(\sigma)$ with the method of least squares.

The electron direct tunneling current density J_G can be expressed in terms of the charge density (N_{ij}) and lifetime (τ_{ij}) of each energy subband in the inversion layer,[11,12] which are functions of stress, σ,

$$J_G(\sigma) = \sum_{i,j} \frac{qN_{ij}(\sigma)}{\tau_{ij}(\sigma)}, \tag{1}$$

where the subscript i denotes Δ_2 (or Δ_4) valley and j each subband belonging to one of these two valleys, respectively. When stress is applied, the change of tunneling current density $\Delta J_G(\sigma)$ is written as

$$\Delta J_G(\sigma) = \sum_{i,j} \left[\frac{\partial J_G}{\partial N_{ij}} \Delta N_{ij}(\sigma) + \frac{\partial J_G}{\partial \tau_{ij}} \Delta \tau_{ij}(\sigma) \right]. \tag{2}$$

Above the threshold voltage, most electrons occupy the lowest two energy states, or each ground state for Δ_2 and Δ_4 valleys. From (2), the relative change of tunneling current due to these two states, $\Delta I_G(\sigma)/I_G(0)$, referenced at zero stress, is calculated as follows, to first order in $\Delta\tau(\sigma)/\tau(0)$:

$$\frac{\Delta I_G(\sigma)}{I_G(0)} \cong A(0)\frac{\Delta N_{\Delta_4}(\sigma)}{N_{\Delta_4}(0)} - B(0)\frac{\Delta \tau_{\Delta_2}(\sigma)}{\tau_{\Delta_2}(0)} - C(0)\frac{\Delta \tau_{\Delta_4}(\sigma)}{\tau_{\Delta_4}(0)}, \tag{3}$$

where

$$A(0) = \frac{-1 + \tau_{\Delta_2}(0)/\tau_{\Delta_4}(0)}{N_{\Delta_2}(0)/N_{\Delta_4}(0) + \tau_{\Delta_2}(0)/\tau_{\Delta_4}(0)},$$

$$B(0) = \frac{N_{\Delta_2}(0)/N_{\Delta_4}(0)}{N_{\Delta_2}(0)/N_{\Delta_4}(0) + \tau_{\Delta_2}(0)/\tau_{\Delta_4}(0)},$$

and

$$C(0) = \frac{N_{\Delta_4}(0)/N_{\Delta_2}(0)}{N_{\Delta_4}(0)/N_{\Delta_2}(0) + \tau_{\Delta_4}(0)/\tau_{\Delta_2}(0)}.$$

Note in the approximation, we use $\Delta N_{\Delta_2}(\sigma) + \Delta N_{\Delta_4}(\sigma) \cong 0$ (neglecting higher subbands) and assume that linear relationships for parameters, τ and N, are valid since the applied stresses are small (<300 MPa). The approximation has been checked numerically and introduced little error. The tunneling lifetimes of the electrons in each Δ_2 and Δ_4 ground state under compressive $\langle 110 \rangle$ stress are given by[11]

$$\tau_{\Delta_2/\Delta_4}(\sigma) = \frac{1}{T_{\Delta_2/\Delta_4}(\sigma)} \frac{\pi\hbar}{E_{\Delta_2/\Delta_4}(\sigma)}, \tag{4}$$

and quantized energy levels, $E_{\Delta_2}(\sigma)$ and $E_{\Delta_4}(\sigma)$, are also given by[13–16]

$$E_{\Delta_2}(\sigma) = \left(\frac{9hqF_{\mathrm{eff},\Delta_2}}{16\sqrt{2m^*_{\Delta_2}}} \right)^{2/3} + \left(\Xi_d + \frac{\Xi_u}{3} \right)(S_{11} + 2S_{12})\sigma + \left(\frac{\Xi_u}{3} \right)(S_{12} - S_{11})\sigma, \tag{5}$$

$$E_{\Delta_4}(\sigma) = \left(\frac{9hqF_{\mathrm{eff},\Delta_4}}{16\sqrt{2m^*_{\Delta_4}}} \right)^{2/3} + \left(\Xi_d + \frac{\Xi_u}{3} \right)(S_{11} + 2S_{12})\sigma - \left(\frac{\Xi_u}{6} \right)(S_{12} - S_{11})\sigma, \tag{6}$$

where $T_{\Delta_2/\Delta_4}(\sigma)$ is the transmission probability of a modified

Downloaded 11 Jan 2007 to 128.227.127.198. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp

WKB method,[11,12] and the quantization effective masses, $m^*_{\Delta_2}=0.92m_0$ and $m^*_{\Delta_4}=0.19m_0$, and the elastic compliance constants, $S_{11}=7.68\times10^{-12}$ m^2/N and $S_{12}=-2.14\times10^{-12}$ m^2/N. In the above expressions, the second and third terms are hydrostatic and shear strain components, respectively, and the stress, σ, has negative values for compression, but the plots (Figs. 2 and 3) are made on a positive scale for convenience. The effective electric fields ($F_{\mathrm{eff},\Delta_2}$ and $F_{\mathrm{eff},\Delta_4}$) are introduced into our model to compensate for triangular potential approximation errors in the inversion condition,

$$F_{\mathrm{eff},\Delta_2/\Delta_4}=\frac{Q_{d,\max}+\eta_{\Delta_2/\Delta_4}Q_{\mathrm{inv}}}{\varepsilon_{\mathrm{Si}}}, \tag{7}$$

where $Q_{d,\max}$ is the maximum depletion sheet charge density, Q_{inv} is the inversion sheet charge density, and $\varepsilon_{\mathrm{Si}}$ is the Si dielectric constant. The correction factors used in our model are $\eta_{\Delta_2}=0.75$ and $\eta_{\Delta_4}=1$.[11,12] Figures 2(b)–2(d) show which terms in (3) contribute to the change in the gate leakage at low and high gate voltages. At low gate biases, the stress-induced repopulation term [the first term in (3)] contributes greatly to tunnel current as shown in Fig. 2(b), while its effect reduces gradually as the gate bias increases as shown in Figs. 2(c) and 2(d). In Fig. 3, two deformation potential constants (Ξ_d and Ξ_u) are used to fit the measured data. The model fits well with the data over the entire range of gate bias (0.4–1.6 V), which encompasses the entire direct tunnel current region.[12] The best fit [$\Delta E_{\Delta_2}(\sigma)\cong-1.705\times10^{-11}\sigma$ eV and $\Delta E_{\Delta_4}(\sigma)\cong2.995\times10^{-11}\sigma$ eV with σ in units of pascal] results in $\Xi_d\cong1.0\pm0.1$ eV and $\Xi_u\cong9.6\pm1.0$ eV. The obtained values of deformation potential constants are very close to theoretical values for bulk Si by Fischetti and Laux ($\Xi_d=1.1$ eV and $\Xi_u=10.5$ eV).[8] The sensitivity to different values of deformation potentials is also shown in Fig. 3. The low gate bias slopes are set by the stress-induced band splitting energy, $\Delta E_{\Delta_4}(\sigma)$. The entire curve is adjusted up or down by the magnitude of the SiO_2/Si barrier height [$\Delta E_{\Delta_2}(\sigma)$] since the change in $\Delta E_{\Delta_2}(\sigma)$ results in a parallel shift without any change in the already determined low gate bias slopes. To illustrate the goodness of the model fit, ±10% deviations in both $\Delta E_{\Delta_2}(\sigma)$ and $\Delta E_{\Delta_4}(\sigma)$ are plotted, in which Ξ_d ranges from 0.873 to 1.141 eV and Ξ_u ranges from 8.61 to 10.5 eV. These fits are shown as the dashed lines in Fig. 3 and significant deviation is observed for 5% differences in the deformation potential constants. Stress effects on the oxide thickness are less than 0.05% at $\sigma=-300$ MPa, assuming SiO_2 contracts the same amount as Si along the stress direction, and has negligible effects on the model prediction and least-squares fit of the deformation potential constants.

In summary, the gate bias dependence on $\Delta I_G(\sigma)/I_G(0)$ as a function of mechanical stress for *n*-MOSFETs has been used to extract the conduction band deformation potential constants. The hydrostatic deformation potential constant, which is traditionally hard to measure, is extracted from the tunneling current and shows excellent agreement with recent numerical calculations.[8,13,14] These values of deformation potential constants suggest that the strain-induced conduction band shift is approximately $E_C(\sigma)=-1.71\times10^{-11}\sigma$ eV for ⟨110⟩ uniaxial strain and $E_C(\sigma)=-3.65\times10^{-11}\sigma$ eV for biaxial strain. The measured conduction band shift in this work is smaller than that typically assumed for biaxial strain, $E_C(\varepsilon)=-14.05\varepsilon$ [or $E_C(\sigma)=-9.04\times10^{-11}\sigma$ eV].[17,18] However, this smaller value of conduction band shift is consistent with both the theoretical calculations[8,13,14] and magnitude of the strain-induced MOSFET threshold voltage shift.[7]

The authors thank and acknowledge the support of an Applied Materials Graduate Fellowship, SRC, and NSF (Grant No. ECS-0524316).

[1] S. E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus, M. Zhiyong, B. Mcintyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. El-Mansy, IEEE Electron Device Lett. **25**, 191 (2004).
[2] V. Chan, R. Rengarajan, N. Rovedo, W. Jin, T. Hook, P. Nguyen, J. Chen, E. Nowak, X. Chen, D. Lea, A. Chakravarti, V. Ku, S. Yang, A. Steegen, C. Baiocco, P. Shafer, H. Ng, S. Huang, and C. Wann, Tech. Dig. - Int. Electron Devices Meet. **2003**, 77.
[3] P. R. Chidambaram, B. A. Smith, L. H. Hall, H. Bu, S. Chakravarthi, Y. Kim, A. V. Samoilov, A. T. Kim, P. J. Jones, R. B. Irwin, M. J. Kim, A. L. P. Rotondaro, C. F. Machala, and D. T. Grider, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **2004**, 48.
[4] S. Thompson, M. Armstrong, C. Auth, B. Arcot, M. Alavi, P. Bai, J. Bielefeld, R. Bigwood, J. Brandenburg, M. Buehler, S. Cea, V. Chikarmane, C. Choi, R. Frankovic, T. Ghani, G. Glass, W. Han, T. Hoffmann, M. Hussein, P. Jacob, A. Jain, C. Jan, S. Joshi, C. Kenyon, J. Klaus, S. Klopcic, J. Luce, Z. Ma, B. Mcintyre, K. Mistry, A. Murthy, P. Nguyen, H. Pearson, T. Sandford, R. Schweinfurth, R. Shaheed, S. Sivakumar, M. Taylor, B. Tufts, C. Wallace, P. Wang, C. Weber, and M. Bohr, Tech. Dig. - Int. Electron Devices Meet. **2002**, 61.
[5] H. Miyata, T. Yamada, and D. K. Ferry, Appl. Phys. Lett. **62**, 2661 (1993).
[6] K. Rim, J. Welser, J. Hoyt, and J. Gibbons, Tech. Dig. - Int. Electron Devices Meet. **1995**, 517.
[7] J. Lim, S. E. Thompson, and J. G. Fossum, IEEE Electron Device Lett. **25**, 731 (2004).
[8] M. Fischetti and S. E. Laux, J. Appl. Phys. **80**, 2234 (1996).
[9] S. E. Thompson, G. Sun, K. Wu, J. Lim, and T. Nishida, Tech. Dig. - Int. Electron Devices Meet. **2004**, 221.
[10] W. Zhao, A. Seabaugh, V. Adams, D. Jovanovic, and B. Winstead, IEEE Electron Device Lett. **26**, 410 (2005).
[11] N. Yang, W. K. Henson, J. R. Hauser, and J. J. Wortman, IEEE Trans. Electron Devices **46**, 1464 (1999).
[12] Y. T. Hou, M. F. Li, Y. Jin, and W. H. Lai, J. Appl. Phys. **91**, 258 (2002).
[13] C. G. Van de Walle and R. M. Martin, Phys. Rev. B **34**, 5621 (1986).
[14] C. G. Van de Walle, Phys. Rev. B **39**, 1871 (1989).
[15] J. Welser, J. Hoyt, S. Takagi, and J. Gibbons, Tech. Dig. - Int. Electron Devices Meet. **1994**, 373.
[16] I. Balslev, Phys. Rev. **143**, 636 (1966).
[17] W. Zhang and J. G. Fossum, IEEE Trans. Electron Devices **52**, 263 (2005).
[18] T. Numata, T. Mizuno, T. Tezuka, J. Koga, and S. Takagi, IEEE Trans. Electron Devices **52**, 1780 (2005).

Downloaded 11 Jan 2007 to 128.227.127.198. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp