

Comparison of Uniaxial Wafer Bending and Contact-Etch-Stop-Liner Stress Induced Performance Enhancement on Double-Gate FinFETs

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Abstract—Longitudinal piezoresistance (π) coefficients for n- and p-type double-gate (DG) FinFETs with sidewall channels along (110) surface and $\langle 110 \rangle$ channel direction are measured via wafer-bending experiments (51.4 and $-37 \times 10^{-11} \text{ Pa}^{-1}$ for n- and p-FinFETs, respectively) and are found to differ from bulk Si (110) (31.2 and $-71.8 \times 10^{-11} \text{ Pa}^{-1}$ for n- and p-Si, respectively). Compressive and tensile contact-etch-stop liners (CESLs) are fabricated on DG FinFETs and are found to induce higher channel stress than in planar MOSFETs, with 30% enhancement in the saturation current for the shortest channel-length devices in both n- and p-MOSFETs, whereas the long devices show little or no enhancement. The channel-length dependence of the enhancement suggests that stress coupling into the FinFET channels from the CESL occurs via the fin extensions and not through the gate.

Index Terms—Contact-etch-stop liners (CESLs), finFET, piezoresistance, wafer bending and strain.

I. INTRODUCTION

NON-PLANAR 3-D devices such as double-gate (DG) FinFETs are considered a possible replacement for planar devices to extend the Si roadmap at 22 nm and beyond [1], [2]. Additional performance enhancement in FinFETs via strain using different types of stressors such as SiGe [3] and SiC [4] source/drain, contact-etch-stop liners (CESLs) [2], [5], [6], global strain engineering [7], [8], and various combinations [1], [9], [10] have been recently investigated. Among the various strain techniques, CESLs are the simplest and most direct way to induce stress into the FinFET channels [6]. Performance enhancement from CESL in planar devices is well understood, but there lacks a quantitative understanding of the same for the FinFET case mainly because most existing strain enhancement models rely on bulk π coefficients [2], [5]–[7], [9], [11]. The first externally applied mechanical stress effect on MuGFETs was reported in [11], but this work was limited to biaxial stress which does not yield the channel π coefficients. In this letter, we measure the longitudinal π coefficients for both n- and

p-FinFETs via uniaxial wafer bending over a 1-GPa stress range and compare them with the bulk π -values. This understanding is further used to explain the stress-transfer mechanism in FinFETs from the CESLs.

II. DEVICE FABRICATION AND EXPERIMENT

FinFETs are fabricated using silicon-on-insulator wafers with 80-nm silicon top layer and 145-nm buried oxide. Fins of width down to 20 nm and gate lengths ranging from 100 nm to 10 μm are patterned with 193-nm lithography and reactive-ion etching. A 2-nm high- k gate dielectric followed by TiN metal gate stack is deposited by atomic layer deposition. This is followed by a 200-nm poly-Si gate deposition using chemical vapor deposition. The gates are patterned and resist etched to form devices with (110) sidewall surfaces and $\langle 110 \rangle$ channel direction. Implanted source/drain dopants are activated by spike anneal, whereas the fins are left undoped. Then, 50-nm tensile and compressive CESLs (t- and c-CESLs, respectively) with built-in stresses of ~ 1 and ~ 1.4 GPa are deposited on n- and p-FinFETs, respectively. The control devices have a very low stress (< 60 MPa) c-CESL. The presence of a SiN hard mask on the top of the fin makes it a DG instead of a trigate FinFET. Tungsten vias and AlSi metal at M1 complete the device processing.

III. RESULTS AND DISCUSSION

A CESL induces stresses in three directions in a FinFET, hence modeling requires three π coefficients: π longitudinal (x), π in-plane transverse (z), and π out-of-plane transverse (y). A schematic diagram of a FinFET with the stress-application direction is shown in the inset of Fig. 1(a). Because of the 3-D nature of the fins and the different aspect ratio of the fin with respect to the Si substrate, there is a lot of uncertainty in estimating the mechanical stress induced in the y - and z -directions. Uniaxial stress application along the channel direction (x) does not suffer from this problem. In order to verify the accuracy of the stress applied by the wafer-bending setup [12], the linear drive-current enhancement of a long (1- μm) channel-length 200-nm-wide n-FinFET is measured versus externally applied stress and is compared with (110)/ $\langle 110 \rangle$ planar n-MOSFET. From Fig. 1(a), we see the expected result that the wide FinFET device, which has negligible physical confinement of the carriers, behaves similar

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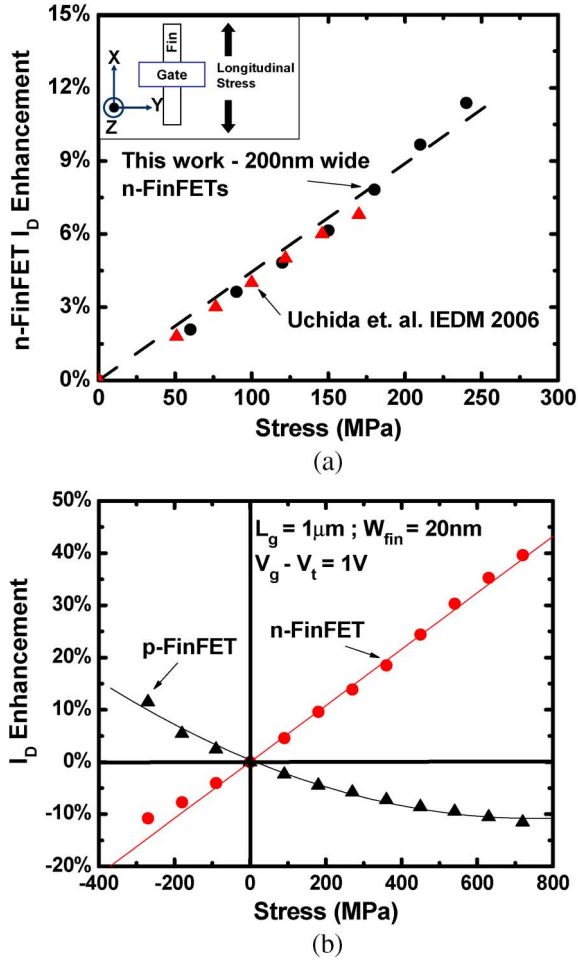


Fig. 1. (a) Drive-current enhancement with uniaxial tensile stress for 1- μm -long 200-nm-wide n-FinFETs compared with published data on planar (110)/(110) n-MOSFETs. Inset shows the schematic of a fin and the stress-application direction. (b) Drive-current enhancement plotted versus uniaxial stress for both n- and p-FinFETs.

to a planar MOSFET and that the longitudinal π value extracted is accurate. With this knowledge, linear and saturation drive-current enhancement is measured on 1- μm -channel-length 20-nm-wide n- and p-FinFET devices for over a 1-GPa stress range and is shown in Fig. 1(b). The extracted longitudinal π coefficients from the wafer-bending data, along with those for planar MOSFETs [13], [14], and bulk values [15], [16] for both n and p-type devices are shown in Table I. The bulk π values differ from those of FinFETs as should be expected due to strong physical and electrical confinement-induced band splitting.

Fig. 2(a) shows the saturation drive-current enhancement of 100-nm-channel-length 20-nm-wide n- and p-FinFETs with t- and c-CESLs, respectively, as compared with the control wafer at a gate overdrive of 0.85 V. The data are averaged over nine sites on the wafer. Both n- and p-FinFET devices show $\sim 30\%$ enhancement which is approximately twice larger than the enhancement of $\sim 15\%$ on planar devices with the same CESL [17]. Using the piezoresistance data in Table I and the enhancement data in Fig. 2(a), a qualitative estimate of an effective channel stress (along x) can be made, but it is not accurate because the actual stress is in all the three directions. Fig. 2(b) shows similar data for 10- μm -channel-length 20-nm-

TABLE I
LONGITUDINAL PIEZORESISTANCE COEFFICIENTS FOR n- AND p-FINFETs ALONG WITH PREVIOUS PUBLISHED DATA FOR PLANAR MOSFETs AND BULK Si (110)

Device Type	Longitudinal Piezoresistance Coefficients (110)/<110>	
	Units ($\times 10^{-11} \text{Pa}^{-1}$)	
	N-type	P-type
FinFET (This Work)	51.4	-37
Planar MOSFET	40 ^[13]	-27.3 ^[14]
Bulk Si (110)	31.2 ^[15, 16]	-71.8 ^[15, 16]

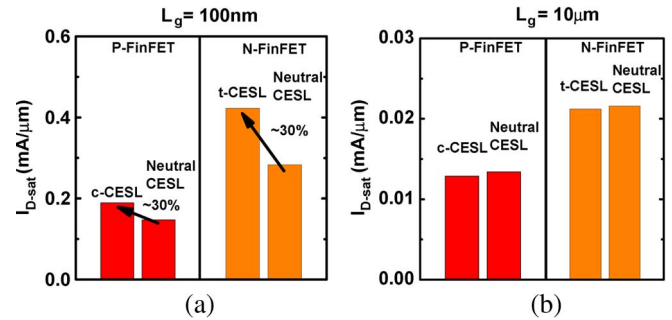


Fig. 2. (a) Saturation I_D - V_g of 100-nm-channel-length 20-nm-wide n- and p-FinFETs with t- and c-CESLs, respectively, along with control at a gate overdrive of 0.85 V. (b) Same for 10- μm devices.

wide FinFETs, which show no enhancement compared to the control devices. This result implies that the stress induced by the CESL has a strong channel-length dependence, which is explained in the next section.

IV. STRESS-TRANSFER MECHANISM

A TEM cross section of the fins, gate stack, and CESL is shown in Fig. 3(a). As observed in the cross section, the CESL is not wrapped around the fin along the gate, and hence, we can expect little stress coupling to take place into the fins through the gate. However, the t-CESL is wrapped directly around the fin at the fin extensions and induces a compressive stress along the y - and z -directions, as shown in the schematic diagram of Fig. 3(b). From wafer-bending results in [13] on planar devices, it is known that compressive stress along y - and z -directions enhances n-MOSFET performance. Because the aforementioned stress coupling takes place along the fin extension, the proximity of the channel to the source/drain fin extensions will be a determining factor for the amount of stress transfer into the channel region under the gate. This is evident from the strong channel-length dependence observed in the performance enhancement due to the CESL where the shortest devices (100 nm) show the maximum performance enhancement of $\sim 30\%$, whereas the long devices (10 μm) show little or no difference from the control wafers. Similar arguments hold for a c-CESL for p-FinFET where a tensile stress is induced along the y - and z -directions which enhance the p-FinFET performance [5].

On the other hand, if the gate is scaled in height to be more conformal, similar arguments would hold true as there would be an additive effect from the stress coupling from the

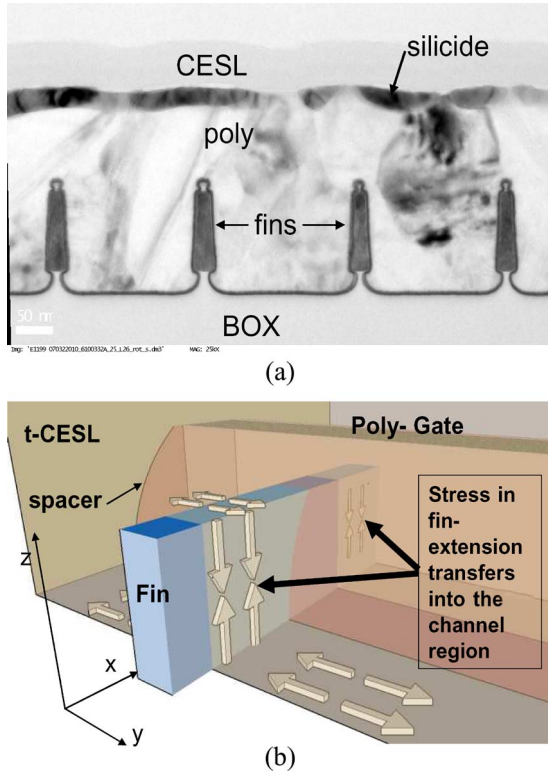


Fig. 3. (a) TEM cross-sectional view of a DG FinFET with a CESL along the gate. (b) Schematic diagram of a FinFET with a CESL along the fin extension. The arrows indicate the direction of stress in the CESL, which is the same as that in the fin.

1) fin extensions and 2) that directly through the gate. Both these factors induce stress into the channel in a similar fashion, although the stress coupling directly through the gate will be channel length independent.

V. CONCLUSION

Wafer-bending experiments show that the FinFET longitudinal π values differ from the bulk π values. CESLs show an almost-twice-larger drive-current enhancement in both n- and p-FinFETs compared with planar MOSFETs due to the stress coupling via the fin extensions. This implies that CESLs are an essential component of future FinFET fabrication processes and can be optimized for further enhancements.

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