Piezoresistance Coefficients of (100) Silicon nMOSFETs Measured at Low and High (∼1.5 GPa) Channel Stress

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***Abstract*—A flexure-based four-point mechanical wafer bending setup is used to apply large uniaxial tensile stress (up to 1.2 GPa) on industrial nMOSFETs with 0 to ∼700 MPa of process-induced stress. This provides the highest uniaxial channel stress to date at ∼1.5 GPa. The stress altered drain–current is measured for long and short (50−140 nm) devices and the extracted π-coefficients are observed to be approximately constant for stresses up to ∼1.5 GPa. For short devices, this trend is seen only after correcting for the significant degradation in the π-coefficients observed due to parasitic source/drain series resistances ($R_{s/d}$).**

***Index Terms*—Piezoresistance, strained-silicon, uniaxial, wafer bending.**

I. Introduction

UNIAXIAL process induced strained-Si has become the preferred method to enhance transistor performance for sub-100-nm technologies [1]–[3]. The magnitude of channel stress in second generation strained-Si technologies (65-nm technology node) [4], [5] is approaching 1 GPa and even higher levels of channel stress will likely be used for the 45 nm and beyond technology nodes. Modeling of the highly strained-Si devices has largely used piezoresistance coefficients, particularly for nMOSFETs, due to the difficulty in predictively modeling the stress enhanced electron mobility [6], [7]. However, nearly all the experimentally determined coefficients are used outside the stress range in which they were extracted and nonlinearity in the piezoresistance should be expected [8]. For example, to model the mobility enhancement in 90- and 65-nm technologies [1], [9], Smith π coefficients [10] are used which were extracted at stresses up to only 10 MPa. Recently, there have been studies [11]–[17] measuring MOSFET piezoresistance coefficient for slightly larger stresses in the range of a few 100 MPa with one exception being Wang *et al.* [16] with nMOSFET data up to ∼580 MPa for long channel and 300 MPa for short channel MOSFETs, all of this still below the high stress levels already in production [1], [9]. In this letter, we extend the stress range and measure piezoresistance coefficients and mobility enhancement at both low and high stresses up to ∼1.5 GPa.

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II. Experiment Setup

To achieve large uniaxial channel stress, the wafer bending experiments have three key elements, namely 1) samples with various amounts of process induced stress and sample preparation, 2) flexure-based four-point bending setup, and 3) stress calibration.

A. Sample Preparation

An important factor for achieving high stress is the quality of the wafer edges used for measurement. To achieve near optical quality wafer edges, wafer cleaving is performed using microposition controlled diamond tip scribes. Other techniques such as laser cutting and edge polishing were tried but resulted in samples that did not obtain > 500 MPa of mechanical stress because of edge defects.

B. Flexure-Based Setup

A flexure-based four-point bending setup used for applying ∼1.2 GPa of uniaxial stress at the top surface of silicon wafers is shown in Fig. 1(a). A flexure is a long beam with a notch on one end, which gives the beam only 1 degree of freedom suppressing the others [18]. The setup has a system of eight such flexure beams which provide uniaxial upward displacement to the bottom rods in a traditional four-point bending setup as shown in the schematic Fig. 1(b). This eliminates error due to uneven rotation of two screws present in traditional four-point bending setups [17], [19] and is essential for achieving high stress.

C. Stress Calibration

The surface stress σ along the channel direction is calculated from the relationship [20]: $\sigma = Eyt/\{2a(L/2 - 2a/3)\}$ where E is the Young's Modulus ($E = 168$ GPa for $\langle 110 \rangle$ channel), y is the sample vertical displacement, t the total thickness of the sample, L is the length of the sample between the two outer rods, and a is the distance between the inner and outer rods as shown in the schematic Fig. 1(b). The setup was calibrated with a load cell under the mounting platform and a strain gauge

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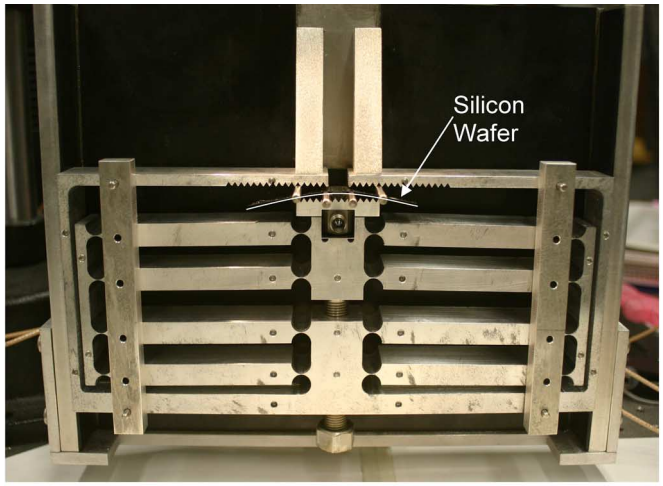
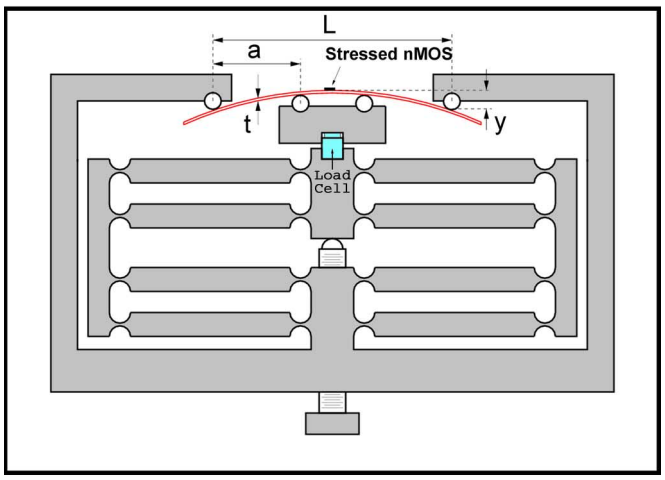
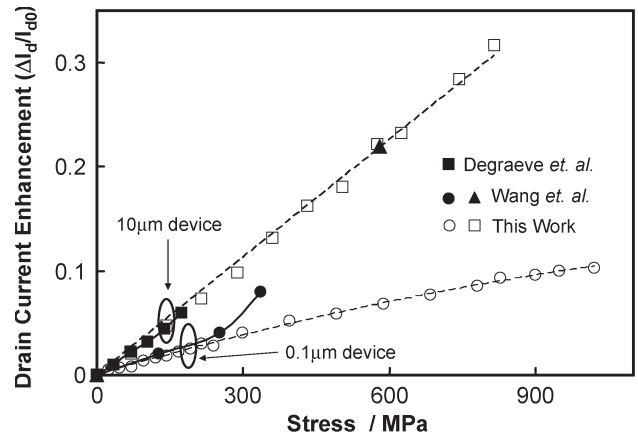


(a)

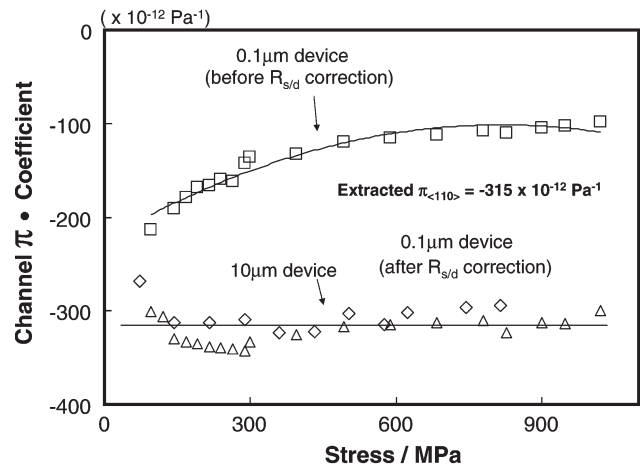


(b)

Fig. 1. Flexure-based wafer bending jig (a) photograph and (b) schematic diagram.



(a)



(b)

Fig. 2. (a) $I_{\mathrm{d-lin}}$ enhancement versus uniaxial longitudinal tensile stress plotted for 10- and 0.1-μm devices along with other published work. (b) Extracted channel π-coefficient values for 10- and 0.1-μm devices (before and after $R_{\mathrm{s/d}}$ correction) plotted versus stress.

mounted on to the surface of the wafer. Provided we used thick $\sim$600 μm samples, these measurements yielded that the actual stress is within 5% error margin of that calculated from the above expression even for stresses up to 1.2 GPa.

The samples used in this letter consist of nMOSFETs with (100) surface, $\langle 110 \rangle$ channel, $\sim$1.2$-$1.4-nm nitrided, SiO_2 gate oxide, phosphorus doped n+ polysilicon gates and body doping density (N_A) $\sim 10^{18}/\mathrm{cm}^3$. The devices either had an unstressed or stressed nitride capping layer creating samples with various amounts of process-induced stress ranging from 300 to 700 MPa ($\pm$100 MPa) for the short devices. The effective process-induced built-in stress is the sum of longitudinal and out-of-plane stress as determined using the relation $\sigma_{\mathrm{eff}} = \sigma_{\langle 110 \rangle} + \pi_{\mathrm{op}}/\pi_{110}\, \sigma_{\langle \mathrm{op} \rangle}$ [21], [10] ("op" stands for out of plane) and two-dimensional FLOOPs stress simulations [22]. The measured devices had the following width/ gate lengths: 10/10, 10/0.1, 1/0.14, and 1/0.05 (in micrometers). Linear drain–current was measured with a Keithley 4200 semiconductor parameter analyzer at $V_{\mathrm{ds}} = 50$ mV and V_{gs} swept from 0 to 1.2 V. All drain–current and mobility enhancement extractions were done at $E_{\mathrm{eff}} \approx 0.7$ MV/cm [23].

III. Results and Discussion

The stress-altered drain–current versus total uniaxial longitudinal stress for long and short devices is shown in Fig. 2(a). Observed is a linear drain–current enhancement for the long devices for longitudinal tensile stresses up to 820 MPa and hence an approximately constant π-coefficient with a value of -315×10^{-12} Pa^{-1} [extracted and plotted in Fig. 2(b)]. Stress-altered short-channel data are also shown for stresses greater than 1 GPa (The stress due to the bending setup is assumed to add linearly to the built-in process stress) in Fig. 2(a) and (b). For the short devices, a nonlinear slope in the drain–current and a considerable degradation in the π-coefficient are observed (with respect to the long devices).

The intrinsic channel π-coefficient values for the short devices ($L_g = 0.14$, 0.1, and 0.05 μm) can be estimated by correcting for the source and drain external resistance $R_{\mathrm{s/d}}$ from the stress altered channel mobility. A simple R_{tot} slope-based effective channel mobility (μ_{eff}) extraction method outlined in [24] is used to correct for the parasitic $R_{\mathrm{s/d}}$ dependence of the short devices. This method offers a simple way of finding μ_{eff} by plotting the R_{tot} for both long- and short-channel devices at a given vertical field versus channel length with the intercept

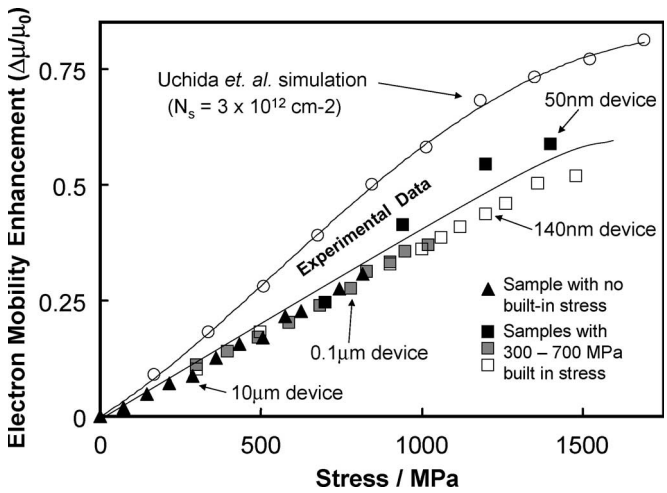


Fig. 3. Extracted effective mobility enhancement ($\mu_{\rm eff}$) versus stress plotted for long and short devices with $R_{\rm s/d}$ correction versus stress at $E_{\rm eff} \approx 0.7$ MV/cm.

of this plot giving us the $R_{\rm s/d}$ (50%–60% of $R_{\rm tot}$ in this letter) contribution to the $R_{\rm tot}$. The total resistance is given by $R_{\rm tot} = V_{\rm ds}/I_{\rm d\text{-}lin}$. For the long devices ($L_g = 10\ \mu$m), $\mu_{\rm eff}$ is defined in the linear region of operation by [23] $\mu_{\rm eff} = I_{\rm ds}L_g/C_{\rm ox}W(V_{\rm gs} - V_t)V_{\rm ds}$ where $I_{\rm ds}$ is the drain–current, L_g is the channel length, $C_{\rm ox} = \varepsilon_{\rm ox}/t_{\rm ox}$ is the gate oxide capacitance per unit area, W is the width of the device, $V_{\rm gs}$, $V_{\rm ds}$, and V_t are the gate bias, drain bias, and the threshold voltage, respectively. The effective mobility enhancement for long and short devices obtained by the above two methods is plotted in Fig. 3 along with more samples with various built in process stresses. It can be seen that after $R_{\rm s/d}$ correction the intrinsic channel π-coefficient values [extracted and plotted in Fig. 2(b)] and mobility enhancement (in Fig. 3) are independent of channel length and are linear even up to a stress of 1.5 GPa.

Even though the underlying physics accounting for the large magnitude of electron enhancement is surprisingly not well understood [7] and has been explained only by *ad hoc* assumptions [6], [7], we can still draw a few conclusions from these results. The linearity and enhancement up to $\sim$1.6 times is similar to what has been observed for biaxial stress [25] even though the maximum mobility enhancement should not be expected to be universal and depends on channel doping (smaller enhancement at higher doping because of ionized impurity scattering). It has recently been suggested that uniaxial stress along $\langle 110 \rangle$ provides a significantly larger enhancement over biaxial tensile stress [17] because of band warping leading to reduced conductivity mass but not all calculations support this conclusion [26]. In this letter, strain induced band warping for longitudinal $\langle 110 \rangle$ stress may play some role in the enhanced mobility since the channel doping used for the 50–140-nm channel length devices is higher than that for most of the wafer-based biaxial stress samples but it appears the effect is not large ($< 20\%$).

IV. Conclusion

After correcting for external resistance, the nMOSFETs intrinsic piezoresistance coefficients and stress enhanced mobility are found to be approximately constant and to increase linearly with stress (up to $\sim$1.5 GPa), respectively. The highest level of channel stress in production logic technologies consist of $\sim$1 GPa for pMOSFETs [4] but only $\sim$500 MPa [4] for n-MOSFETs. Thus, the piezoresistance and mobility data suggest stress enhanced electron mobility is not saturated and additional performance enhancement via higher levels of channel stress are possible up to 1.6 times even for high $\sim 10^{18}$ cm^{-3} channel doping. However, to realize the additional electron mobility enhancement at high stress on short devices, the external resistance needs to be reduced. Furthermore, this letter highlights that for nanoscale MOSFETs in logic applications, the real limiter will likely be external resistance and not the magnitude of channel mobility.

References

[1] S. E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus, Z. Ma, B. Mcintyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. El-Mansy, "A logic nanotechnology featuring strained-silicon," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 191–193, Apr. 2004.

[2] V. Chan, R. Rengarajan, N. Rovedo, W. Jin, T. Hook, P. Nguyen, J. Chen, E. Nowak, X. Chen, D. Lea, A. Chakravarti, V. Ku, S. Yang, A. Steegen, C. Baiocco, P. Shafer, H. Ng, S. Huang, and C. Wann, "High speed 45 nm gate length CMOSFETs integrated into 90 nm bulk technology incorporating strain engineering," in *IEDM Tech. Dig.*, Dec. 2003, pp. 3.8.1–3.8.4.

[3] P. R. Chidambaram, A. Smith, L. H. Hall, H. Bu, S. Chakravarti, Y. Kim, A. V. Samoilov, A. T. Kim, P. J. Jones, R. B. Irwin, M. J. Kim, A. L. P. Rotondaro, C. F. Machala, and D. T. Grider, "35% drive current improvement from recessed-SiGe drain extensions on 37 nm gate length PMOS," in *VLSI Symp. Tech. Dig.*, Jun. 2004, pp. 48–49.

[4] C. H. Jan, P. Bai, J. Choi, G. Curello, S. Jacobs, J. Jeong, K. Johnson, D. Jones, S. Klopcic, J. Lin, N. Lindert, A. Lio, S. Natarajan, J. Neirnyck, P. Packan, J. Park, I. Post, M. Patel, S. Ramey, P. Reese, L. Rockford, A. Roskowski, G. Sacks, B. Turkot, Y. Wang, L. Wei, J. Yip, I. Young, K. Zhang, Y. Zhang, M. Bohr, and B. Holt, "A 65 nm ultra low power logic platform technology using uni-axially strained-silicon transistors," in *IEDM Tech. Dig.*, Dec. 2005, pp. 60–63.

[5] A. Steegen, R. Mo, R. Mann, M.-C. Sun, M. Eller, G. Leake, D. Vietzke, A. Tilke, F. Guarin, A. Fischer, T. Pompl, G. Massey, A. Vayshenker, W. L. Tan, A. Ebert, W. Lin, W. Gao, J. Lian, J.-P. Kim, P. Wrschka, J.-H. Yang, A. Ajmera, R. Knoefler, Y.-W. Teh, F. Jamin, J. E. Park, K. Hooper, C. Griffin, P. Nguyen, V. Klee, V. Ku, C. Baiocco, G. Johnson, L. Tai, J. Benedict, S. Scheer, H. Zhuang, V. Ramanchandran, G. Matusiewicz, Y.-H. Lin, Y. K. Siew, F. Zhang, L. S. Leong, S. L. Liew, K. C. Park, K.-W. Lee, D. H. Hong, S.-M. Choi, E. Kaltalioglu, S. O. Kim, M. Naujok, M. Sherony, A. Cowley, A. Thomas, J. Sudijohno, T. Schiml, J.-H. Ku, and I. Yang, "65 nm CMOS technology for low power applications," in *IEDM Tech. Dig.*, 2005, pp. 64–67.

[6] M. V. Fischetti, F. Gamiz, and W. Hansch, "On the enhanced electron mobility in strained-silicon inversion layers," *J. Appl. Phys.*, vol. 92, no. 12, pp. 7320–7324, Dec. 2002.

[7] S. Takagi, J. J. Hoyt, J. J. Welser, and J. F. Gibbons, "Comparative study of phonon-limited mobility of two-dimensional electrons in strained and unstrained-Si metal-oxide-semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 80, no. 3, pp. 1567–1577, Aug. 1996.

[8] M. V. Fischetti, Z. Ren, P. M. Solomon, M. Yang, and K. Rim, "Six-band k.p calculation of the hole mobility in silicon inversion layers: Dependence on surface orientation, strain, and silicon thickness," *J. Appl. Phys.*, vol. 94, no. 2, pp. 1079–1094, Jul. 2003.

[9] T. Irisawa, T. Numata, T. Tezuka, K. Usuda, N. Hirashita, N. Sugiyama, E. Toyoda, and S. Takagi, "High current drive SGOI pMOSFETs fabricated by lateral strain relaxation technique," in *VLSI Symp. Tech. Dig.*, Jun. 2005, pp. 178–179.

[10] C. S. Smith, "Piezoresistance effect in germanium and silicon," *Phys. Rev.*, vol. 94, no. 1, pp. 42–49, Apr. 1954.

[11] A. T. Bradley, R. C. Jaeger, J. C. Suhling, and K. J. O'Connor, "Piezoresistive characteristics of short-channel MOSFETs on (100) silicon," *IEEE Trans. Electron Devices*, vol. 48, no. 9, pp. 2009–2015, Sep. 2001.

[12] C. Gallon, G. Reimbold, G. Ghibaudo, R. A. Bianchi, R. Gwoziecki, S. Orain, E. Robilliart, C. Raynaud, and H. Dansas, "Electrical analysis

of mechanical stress induced by STI in short MOSFETs using externally applied stress," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1254–1261, Aug. 2004.

[13] A. Lochtefeld and D. A. Antoniadis, "Investigating the relationship between electron mobility and velocity in deeply scaled NMOS via mechanical stress," *IEEE Electron Device Lett.*, vol. 22, no. 12, pp. 591–593, Dec. 2001.

[14] R. Degraeve, G. Groeseneken, I. D. Wolf, and H. E. Maes, "The effect of externally imposed mechanical stress on the hot-carrier-induced degradation of deep-sub micron nMOSFET," *IEEE Trans. Electron Devices*, vol. 44, no. 6, pp. 943–950, Jun. 1997.

[15] H. Irie, K. Kita, K. Kyuno, and A. Toriumi, "In-plane mobility anisotropy and universality under uni-axial strains in n- and p-MOS inversion layers on (100), (110), and (111) Si," in *IEDM Tech. Dig.*, Dec. 2004, pp. 225–228.

[16] Y. G. Wang, D. B. Scott, Y. Wu, J. L. Waller, J. Hu, K. Liu, and V. Ukraintsev, "Effects of uniaxial mechanical stress on drive current of 0.13 μm MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 2, pp. 529–531, Feb. 2003.

[17] K. Uchida, T. Krishnamohan, K. C. Saraswat, and Y. Nishi, "Physical mechanisms of electron mobility enhancement in uniaxial stressed MOSFETs and impact of uniaxial stress engineering in ballistic regime," in *IEDM Tech. Dig.*, Dec. 2005, pp. 129–132.

[18] S. T. Smith, *Flexure, Elements of Elastic Mechanisms*. New York: Gordon and Breach, 2000.

[19] S. E. Thompson, G. Sun, K. Wu, J. Lim, and T. Nishida, "Key differences for process-induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs," in *IEDM Tech. Dig.*, Dec. 2004, pp. 221–225.

[20] S. Timoshenko, *Strength of Materials*, 3rd ed. Melbourne, FL: Krieger, 1976. c1958.

[21] L. Smith, V. Moroz, G. Enemen, P. Verheyen, F. Nouri, L. Washington, M. Jurczak, O. Penzin, D. Pramanik, and K. De Mayor, "Exploring the limits of stress-enhanced hole mobility," *IEEE Electron Device Lett.*, vol. 26, no. 9, pp. 652–654, Sep. 2005.

[22] N. Shah, "Stress modeling of nanoscale MOSFET," M.S. thesis, Univ. Florida, Gainesville, 2005.

[23] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge, U.K.: Cambridge Univ. Press, 1998.

[24] G. Niu, J. D. Cressler, S. J. Mathew, and S. Subbanna, "A total resistance slope-based effective channel mobility extraction method for deep submicrometer CMOS technology," *IEEE Trans. Electron Devices*, vol. 46, no. 9, pp. 1912–1914, Sep. 1999.

[25] J. L. Hoyt, H. M. Nayfeh, S. Eguchi, I. Aberg, G. Xia, T. Drake, E. A. Fitzgerald, and D. A. Antoniadis, "Strained-silicon MOSFET technology," in *IEDM Tech. Dig.*, Dec. 2002, pp. 23–26.

[26] P. R. Chidambaram, C. Bowen, S. Chakravarthi, C. Machala, and R. Wise, "Fundamentals of silicon material properties for successful exploitation of strain engineering in modern CMOS manufacturing," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 944–964, May 2006.